Rao Bahadur Y. Mahabaleswarappa Engineering College, Ballari
Department of Electronics & Communication Engineering

COURSE FILE

Academic Year: 2020-21 **(ODD/EVEN)**

Faculty Name	Mrs. ASHWINI.K			
Course Name	Basic Electronics			
Course Code	18ELN24			
Sem/Sec	II / B			
Verified By				

CONTENT

VISION AND MISSION OF THE INSTITUTE AND DEPARTMENT

VISION OF THE INSTITUTION

To Produce Professionally Excellent, Knowledgeable, Globally Competitive and Socially Responsible Engineers and Entrepreneurs.

MISSION OF THE INSTITUTION

M1	To Provide Quality Education in Engineering and Management.
M2	To Establish a Continuous Industry-Institute Interaction, Participation and Collaboration to Contribute Skilled Engineers.
M3	To Develop Human Values, Social Values, Entrepreneurship Skills and Professional Ethics among the Technocrats.
M4	To Focus on Innovation and Development of Technologies by Engaging in Cutting Edge Research areas.

VISION OF THE DEPARTMENT

To Produce Professionally Excellent, Knowledgeable, Globally Competitive and Socially Responsible Electronics and Communication Engineers and Entrepreneurs.

MISSION OF THE DEPARTMENT

M1	To Provide Quality Education in Electronics and Communication Engineering.
M2	To Establish a Continuous Industry-Institute Interaction, Participation and Collaboration to Contribute Skilled Electronics and Communication Engineers.
M3	To Develop Human Values, Social Values, Entrepreneurship Skills and Professional Ethics among the Technocrats.
M4	To Focus on Innovation and Development of Technologies by Engaging in Electronics and Communication Research areas.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1	Graduates of Electronics & Communication Engineering course will have successful professional career.
PEO2	Graduates of Electronics & Communication Engineering course will pursue higher education or to become an Entrepreneur.
PEO3	Graduates of Electronics & Communication Engineering course will have ability for lifelong learning and to serve the society.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO 1	Ability to Design, Develop and Test the Electronics Circuits & Communication Systems.
PSO 2	Ability to Develop Excellent Programming and Problem Solving skills in the field of Embedded System.

PROGRAM OUTCOMES (PO)

PO 1	Engineering Knowledge	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	Problem Analysis	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	Design/ Development of Solutions	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	Modern tool usage	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	The engineer and society	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	Environment and sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	Individual and team work	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	Communication	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	Project management and finance	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	Life-long learning	Recognize the need for, and have the preparation and ability to engage in Independent and life-long learning in the broadest context of technological change.

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

Name of the Staff: Vinay A, Sharna gouda patil,Prashanth Keni,Sudharshan B,Aswini.k.				
Course Name: BASIC ELECTRONICS				
Course Code: 18ELN14	Sem:	1	Year	2020-21

COURSE OUTCOME STATEMENTS	
	At the end of the course, students will be able to ....
C128.1	Summarize the operation, characteristics of diodes, FETs, SCR, Operational amplifiers, IC regulators, astable oscillator using 555 timers and Communication Systems.(L2)
C128.2	Explain the applications of diodes, BJT, SCR, and Operational amplifiers.(L2)
C128.3	Interpret Oscillators and feedback amplifiers.(L2)
C128.4	Explain the different types of number systems; construct the combinational and sequential circuits using flip flops.(L2)

CO-PO/PSO Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
C128.1	3	2												
C128.2	3	2												
C128.3	3	2												
C128.4	3	2												
AVG	3	2												

CO	PO	BTL	Mapping	Justification	Action Verbs	Hours
C128.1	PO1	L1, L2	3	Characteristics of diodes, FETs, SCR contribute to Engineering basics .	Define, Explain, Outline	12 out of 50
	PO2		2	Operational amplifiers, IC regulators, astable oscillator using 555 timers and Communication Systems contribute to Problem Analysis.		
C128.2	PO1	L1 L2,	3	Applications of diodes, BJT, SCR, and Operational amplifiers contribute to Engineering basics .	What, Outline, Explain, Find	13 out of 50
	PO2		2	Applications of diodes, BJT, SCR, and Operational amplifiers contribute to Problem Analysis.		
C128.3	PO1	L2	3	Oscillators and feedback amplifiers contribute to Engineering basics .	Explain	13 out of 50
	PO2		2	Oscillators and feedback amplifiers contribute to Problem Analysis.		
C128.4	PO1	L1, L2,	3	Number systems , flip flops contribute to Engineering basics .	Compare, Recall Explain, Find	12 out of 50
	PO2		2	Number systems , flip flops contribute to Problem Analysis.		

Note:

4 Hours of 50 Hours Mapping Strength is 1

8 Hours of 50 Hours Mapping Strength is 2

12 Hours of 50 Hours Mapping Strength is 3

Course Coordinator

Staff Signature

Academic Calendar of EVEN Semesters of UG Programmes

Semesters / EVENTS	IV semester B.E./B.Tech.	IV semester B.Arch./ B.Plan.	VI semester B.E./B.Tech.	VI semester B.Plan./B.Arch	VIII semester B.E./B.Tech.	VII semester B.Plan./B.Arch.
Commencement of EVEN Semester	19.04.2021	19.04.2021	19.04.2021	19.04.2021	19.04.2021	19.04.2021
Last Working day of EVEN Semester	07.08.2021	07.08.2021	07.08.2021	07.08.2021	20.07.2021	20.07.2021
Practical Examinations	09.08.2021 To 19.08.2021	09.08.2021 To 19.08.2021	09.08.2021 To 19.08.2021	---	---	---
Theory Examinations	23.08.2021 To 09.09.2021	23.08.2021 To 09.09.2021	23.08.2021 To 09.09.2021	10.08.2021 To 31.08.2021	#22.07.2021 To 30.07.2021	#22.07.2021 To 30.07.2021
Internship	—	—	—	—	—	—
Internship Viva-Voce	—	—	—	—	02.08.2021 To 06.08.2021	—
Professional training / Organization study	—	—	—	—	—	—
Commencement of ODD Semester	13.09.2021	13.09.2021	13.09.2021	13.09.2021	—	09.08.2021 (IX sem Arch)

- The classroom sessions for even the semester should commence from the dates mentioned above. The classroom sessions for all the semesters would be in **Offline /Online/blended mode** until further orders.
- The Institute needs to function for **six days** a week with additional hours **(Saturday is a full working day).** #if required the college can plan to have extra classes even on **Sundays also**.
- If any of the above dates are declared to be a holiday then the corresponding event will come into effect on the next working day.
- Notification regarding the Calendar of Events relating to the conduct of **University Examinations** will be issued by the Registrar (Evaluation) from time to time.
- The faculty/staff shall be available to undertake any work assigned by the University.
- Academic Calendar may be modified based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Revised Academic Calendar is also applicable for **Autonomous Colleges.** In case if any changes are to be affected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.

6/6/2024.

REGISTRAR

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI-583104

CALENDAR OF EVENTS 2020-21 SECOND SEMESTER: MAY 2021 TO SEPTEMBER 2021

DATE	MAY	DATE	JUNE	DATE	JULY	DATE	AUGUST	DATE	SEPTEMBER
1		1	TUESDAY					1	WEDNESDAY
2		2	WEDNESDAY			2	MONDAY	2	THURSDAY
3		3	THURSDAY			3	TUESDAY	3	FRIDAY
4		4	FRIDAY			4	WEDNESDAY	4	SATURDAY
5		5	SATURDAY	5	MONDAY				
6				6	TUESDAY			6	MONDAY
7		7	MONDAY	7	WEDNESDAY			7	TUESDAY
8		8	TUESDAY	8	THURSDAY			8	WEDNESDAY
9		9	WEDNESDAY	9	FRIDAY	9	MONDAY	9	THURSDAY
10		10	THURSDAY			10	TUESDAY	10	FRIDAY
11		11	FRIDAY			11	WEDNESDAY	11	SATURDAY
12		12	SATURDAY	12	MONDAY	12	THURSDAY		
13				13	TUESDAY	13	FRIDAY	13	MONDAY
14		14	MONDAY	14	WEDNESDAY			14	TUESDAY
15		15	TUESDAY	15	THURSDAY			15	WEDNESDAY
16		16	WEDNESDAY	16	FRIDAY	16	MONDAY	16	THURSDAY
17		17	THURSDAY			17	TUESDAY	17	FRIDAY
18		18	FRIDAY			18	WEDNESDAY	18	SATURDAY
19	WEDNESDAY	19	SATURDAY	19	MONDAY	19	THURSDAY		
20	THURSDAY			20	TUESDAY	20	FRIDAY		
21	FRIDAY	21	MONDAY	21	WEDNESDAY				
22	SATURDAY			22	THURSDAY				
		23		23	FRIDAY	23	MONDAY	23	THURSDAY
24	MONDAY	24		24	SATURDAY	24	TUESDAY	24	FRIDAY
25	TUESDAY	25				25	WEDNESDAY	25	SATURDAY
26	WEDNESDAY	26	Classes Commence	26	MONDAY	26	THURSDAY		
27	THURSDAY	27	Registration (Form-2)	27	TUESDAY	27	FRIDAY	27	MONDAY
28	FRIDAY	28	Commencement of Class	28	WEDNESDAY	28	SATURDAY	28	TUESDAY
29	SATURDAY	29		29	THURSDAY			29	WEDNESDAY
		30		30	FRIDAY	30	MONDAY	30	Last working day
31	MONDAY			31	SATURDAY	31	TUESDAY		

SL.No.	COMMENCEMENT	LAST WORKING DAY	PRACTICAL EXAM	THEORY EXAM
1	24/05/2021	30/09/2021	04/10/2021 TO 09/10/2021	11/10/2021 TO 21/10/2021

EVEN SEMESTER WILL COMMENCE FROM NOV 15, 2021

HOD

PRINCIPAL

RaoBahadur Y Mahabaleswarappa Engineering College, Ballari

Department of Electronics and Communication Engineering

Academic Calendar of Events
EVEN Semester 2020-21(April 2021-Sept 2021)

	III, V& VII Sem B.E/B.Tech
Pre Placement Training	For VI Semester Students of all Branches from 20th to 25th Sep 2021
Commencement of ODD Semester	19th April 2021
Admission Publicity in and around Ballari	March 2021
Six Days National Webinar on **"Intellectual Property Rights and IP Management for Start - up"** by Mrs. Priyadarshini Singh ,Research Scholar	26th April to 1st may
I Internal Assessment Test	10th, 11th & 12th June 2021 (Thu, Fri & Sat-Online)
Last date for sending IA Marks (SMS)	14st June 2021
Parents Meet	15h June 2021
2nd International Virtual Conference on **"Futuristic Trends in Embedded Systems and Networking" ICFTEN 2021** in association with IFERP and RYMEC	7th-8th July 2021
II Internal Assessment Test	16th, 17th & 18th July 2021 (Tue, Wed & Thu-Online)
Last date for sending IA Marks (SMS)	19th July 2021
Parents Meet	20th July 2021
Department forum "Talentronics"	2nd August 2021
Current Covid 19 Situation and How to Overcome All Diseases by Dr. Khadar Vali	2nd August 2021
Mini project exhibition for 8th sem students	4th august 2021
Farewell day for final year students	8th August 2021
Six Days Workshop on **Basics of Machine Learning using Python**	30th August to 4th Sept 2021
III Internal Assessment Test	12th,13th &14th August 2021(Thu, Fri & Sat-Online)
Last date for sending IA Marks (SMS)	15th August 2021
Mini project exhibition for 6th sem students	18th august 2021
Parents Meet	16th August 2021
Last Working Day	**07/08/2021**
Practical Examination	09/08/2021 to 19/08/2021
Theory Examination	23/08/2021 to 09/09/2021
NBA SAR audit by Ms. Manisha .	7th Sept 2021
NAAC Presentation by DR H Girish ,Coordinator and Dean	13th Sept 2021
Commencement of EVEN Semester	**13/09/2021**

Head of the Department
Electronics & Communication Engg.
R. Y. M. Engineering College,
(Formerly Vijayanagar Engg. College)
HOD ECE
BELLARY-583 104.

BASIC ELECTRONICS

Semester	**: I/II**	**CIE Marks**	**: 40**
Course Code	**: 18ELN14/24**	**SEE Marks**	**: 60**
Teaching Hours/week (L:T:P)	**: 2:2:0**	**Exam Hours**	**: 03**
	Credits : 03		

Course Objectives:

This course will enable students to:

- Understand characteristics, operation and applications of the diodes, bipolar junction transistors, field effect transistors, SCRs and operational amplifiers in electronic circuits.
- Understand different number systems and working of fundamental building blocks of digital circuits.
- Understand the principle of basic communication system and mobile phones.

MODULE-1

Semiconductor Diodes and Applications:

p-n junction diode, Equivalent circuit of diode, Zener Diode, Zener diode as a voltage regulator, Rectification-Half wave rectifier, Full wave rectifier, Bridge rectifier, Capacitor filter circuit (2.2, 2.3, 2.4 of Text 1).

Photo diode, LED, Photo coupler. (2.7.4, 2.7.5, 2.7.6 of Text 1).

78XX series and 7805 Fixed IC voltage regulator (8.4.4 and 8.4.5 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-2

FET and SCR:

Introduction, JFET: Construction and operation, JFET Drain Characteristics and Parameters, JFET Transfer Characteristic, Square law expression for I_D, Input resistance, MOSFET: Depletion and Enhancement type MOSFET-Construction, Operation, Characteristics and Symbols, (refer 7.1, 7.2, 7.4, 7.5 of Text 2). CMOS (4.5 of Text 1).

Silicon Controlled Rectifier (SCR) – Two-transistor model, Switching action, Characteristics, Phase control application (refer 3.4 upto 3.4.5 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-3

Operational Amplifiers and Applications:

Introduction to Op-Amp, Op-Amp Input Modes, Op-Amp Parameters-CMRR, Input Offset Voltage and Current, Input Bias Current, Input and Output Impedance, Slew Rate (12.1, 12.2 of Text 2).

Applications of Op-Amp - Inverting amplifier, Non-Inverting amplifier, Summer, Voltage follower, Integrator, Differentiator, Comparator (6.2 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-4

BJT Applications, Feedback Amplifiers and Oscillators:

BJT as an amplifier, BJT as a switch, Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay (refer 4.4 and 4.5 of Text 2).

Feedback Amplifiers – Principle, Properties and advantages of Negative Feedback, Types of feedback, Voltage series feedback, Gain stability with feedback (7.1-7.3 of Text 1).

Oscillators – Barkhaunsen's criteria for oscillation, RC Phase Shift oscillator, Wien Bridge oscillator (7.7-7.9 of Text 1).

IC 555 Timer and Astable Oscillator using IC 555 (17.2 and 17.3 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-5

Digital Electronics Fundamentals:

Difference between analog and digital signals, Number System-Binary, Hexadecimal, Conversion- Decimal to binary, Hexadecimal to decimal and vice-versa, Boolean algebra, Basic and Universal Gates, Half and Full adder, Multiplexer, Decoder, SR and JK flip-flops, Shift register, 3 bit Ripple Counter (refer 10.1-10.7 of Text 1).

Basic Communication system, Principle of operations of Mobile phone (refer 18.2 and 18.18 of Text 1).

(RBT Levels : L1 & L2)

Course Outcomes:

After studying this course, students will be able to:

- Describe the operation of diodes, BJT, FET and Operational Amplifiers.
- Design and explain the construction of rectifiers, regulators, amplifiers and oscillators.
- Describe general operating principles of SCRs and its application.
- Explain the working and design of Fixed voltage IC regulator using 7805 and Astable oscillator using Timer IC 555.
- Explain the different number system and their conversions and construct simple combinational and sequential logic circuits using Flip-Flops.
- Describe the basic principle of operation of communication system and mobile phones.

Proposed Activities to be carried out for 10 marks of CIE:

Students should construct and make the demo of the following circuits in a group of 3/4 students:

1. +5V power supply unit using Bridge rectifier, Capacitor filter and IC 7805.
2. To switch on/off an LED using a Diode in forward/reverse bias using a battery cell.
3. Transistor switch circuit to operate a relay which switches off/on an LED.
4. IC 741 Integrator circuit/ Comparator circuit.
5. To operate a small loud speaker by generating oscillations using IC 555.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Textbooks:

1. D.P.Kothari, I.J.Nagarath, "Basic Electronics", 2nd edn, Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

Reference Books:

1. D.P.Kothari, I.J.Nagarath, "Basic Electronics", 1st edn, Mc Graw Hill, 2014.
2. Boylestad, Nashelskey, "Electronic Devices and Circuit Theory", Pearson Education, 9th Edition, 2007/11th edition, 2013.
3. David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 5th Edition, 2008.
4. Muhammad H. Rashid, "Electronics Devices and Circuits", Cengage Learning, 2014.

V V SANGHA'S

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI,583104

ACADEMIC YEAR 2020-2021

TIME TABLE FOR II SEMESTER (CHEMISTRY GROUP)

W.E.F : 6-09-2021 **SECTION : B** **ONLINE MODE**

TIME	09:30 AM to 10:30 AM		11:00 AM to 12.00 Noon		12:30 PM to 01:30 PM	1:30 PM to 02:30 PM	02:30 PM to 03:30 PM		04:00 PM to 05:00 PM
Monday	ENG		MAT		CHE		CPS		ELN
Tuesday	MAT		CHE		CPS		ELN		ME
Wednesday	CHE	break	CPS	break	ELN	LUNCH BREAK	ME	break	MAT
Thursday	CPS		ELN		ME		MAT		CHE
Friday	ELN		ME		MAT		CHE		ENG
Saturday	ME		CPS		Mentor & Mentee Talk		Free		

COURSE CODE	COURSE TITLE	STAFF NAME	MOB NO.	EVENTS AND IMPORTANT DATES	
18MAT21	Advanced Calculus and Numerical Methods	Dr. PHAKIRAPPA / Dr. VEERESH	9740145480 /9449632718	Comencment of 2nd semester	19/05/2021
18CHE22	Engineering Chemistry	Mr. K.M.GURUDEVA SHARMA	9449135934	First I.A.Test	01-07-2021 TO 03-07-2021
18CPS23	C Programming for Problem Solving	Mr. PUNEETH G J	9036955271	Second I.A.Test	17-09-2021 TO 19-09-2021
18ELN24	Basic Electronics	MrS. ASHWINI K	9449546469	Third I.A.Test	28-09-2021 TO 30-09-2021
18ME25	Elements of Mechanical Engineering	Mr. B BASAVA PRAKASH	9449614173	Note : Due to Covid Pandemic, First semester exam was conducted in the month July-Aug. 19/07/2021 to 13/08/2021 was declared as study holiday and conduction of exam. 2nd semester resumed from 11th Aug 2021. 11/08/2021 to 04/09/2021 off-line Lab/Theory have been conducted.	
18EGH28	Technical English– II	Ms. PUSHPA B M	9741801538		

02/08/21

19/8/21

R.V. [illegible] College,
(Formerly Vijayanagar Engg. College)
Cantonment, BALLARI-583 104.

RAO BAHADUR Y.MAHABALESWARAPPA ENGINEERING COLLEGE.BALLARI
ACADEMIC YEAR 2020-21 EVEN SEMESTER

ONLINE CLASSES SCHEDULE FOR SECOND SEMESTER

W.E.F 29-04-2021

SEMESTER-II (Chemistry Group: Sec: A, B,C,D,E)			
TIME	10:30 AM TO 11.30AM	12:30PM TO 01:30PM	3:30PM TO 4:30PM
MONDAY	BE	MAT	CPS
TUESDAY	CHE	CPS	MAT
WEDNESDAY	CPS	BE	CHE
THURSDAY	MAT	CHE	ME
FRIDAY	ME	CPS	BE
SATURADAY	MAT	BE	ME

SEMESTER-II (Chemistry Group) For Technical English-II	
TIME	5:00 PM TO 6.00PM
MONDAY	Sec A & B
TUESDAY	Sec C & D
WEDNESDAY	Sec E

SL NO	SUB-CODE	SUBJECT NAME
1	18MAT21	Advanced Calculus and Numerical Methods
2	18CHE22	Engineering Chemistry
3	18CPS23	C Programming for Problem Solving
4	18ELN24	Basic Electronics
5	18ME25	Elements of Mechanical Engineering
6	18EGH28	Technical English-II

First Year Co-ordinator

HEAD
Department of Mathematics,
R.Y. Engineering College,
(Formerly, Engg. College).

Principal

V.V.Sangha's

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics & Communication Engineering

Time Table

Staff Name: ASHWINI.K	**Sem :** II **Sec:** B
Course Name: Basic Electronics	**Course Code:** 18ELN24
Lab Name:	**Code:**

Day	9am-9:55am	9:55am-10:50am	10:50am-11:00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
Monday		10.30 - 11.30 ELN							
Tuesday			BREAK			BREAK			
Wednesday					12.30 - 01.30pm ELN				
Thursday									
Friday								3.30 - 4.30 Pm ELN	
Saturday					12.30 - 1.30 ELN				

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

COURSE PLAN 2020-21 (EVEN)

Staff Name: Ashwini K	**Course Type: Core**	**Sem / Sec: II/B**
Course Name: Basic Electronics	**Course Code: 18ELN24**	**Total Number of Lecture Hours:60**
Max marks: 100	**Prerequisites: Physics, Mathematics**	

Sl. No	Module Name	Lecture Hours Required
01	MODULE-1 : SEMICONDUCTOR DIODES AND APPLICATIONS	14
02	MODULE-2 : FET and SCR	11
03	MODULE-3 : OPERATIONAL AMPLIFIERS AND APPLICATIONS	12
04	MODULE-4 : BJT APPLICATIONS, FEEDBACK AMPLIFIERS AND OSCILLATORS	13
05	MODULE-5 : DIGITAL ELECTORNICS FUNDAMENTALS	10

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

Sl.No	Date	Time	Topic to be Covered
MODULE-1 : SEMICONDUCTOR DIODES AND APPLICATIONS			
1.	30/4/2021	3.30PM-4.30PM	P-N Junction Diode
2.	1/5/2021	12.30PM-1.30PM	Equivalent circuit of diode
3.	5/5/2021	12.30PM-1.30PM	Zener Diode. Zener diode as a voltage regulator
4.	5/5/2021	12.30PM-1.30PM	Rectification-Half Wave rectifier
5.	7/5/2021	3.30PM-4.30PM	Full wave rectifier
6.	8/5/2021	12.30PM-1.30PM	Problems
7.	10/5/2021	10.30AM-11.30AM	Bridge Rectifier
8.	12/5/2021	12.30PM-1.30PM	Problems
9.	14/5/2021	3.30PM-4.30PM	Capacitor Filter Circuit
10.	15/5/2021	12.30PM-1.30PM	Photo diode. LED
11.	17/5/2021	10.30AM-11.30AM	Photo Coupler.
12.	19/5/2021	12.30PM-1.30PM	78XX Series
13.	21/5/2021	3.30PM-4.30PM	7805 Fixed IC Voltage regulator
14.	22/5/2021	12.30PM-1.30PM	Problems
MODULE-2 : FET and SCR			
15.	24/5/2021	10.30AM-11.30AM	Introduction . JFET: Construction and Operation
16.	26/5/2021	12.30PM-1.30PM	JFET Drain Characteristics and Parameters
17.	28/5/2021	3.30PM-4.30PM	JFET Transfer Characteristic
18.	29/5/2021	12.30PM-1.30PM	Square Law Expression for I_D , Input Resistance
19.	31/5/2021	10.30AM-11.30AM	MOSFET: Depletion type Mosfet Construction, Operation.
20.	2/6/2021	12.30PM-1.30PM	MOSFET Characteristics and symbols
21.	4/6/2021	3.30PM-4.30PM	MOSFET: Enhancement Type Mosfet Construction.
22.	5/6/2021	12.30PM-1.30PM	MOSFET: Enhancement Operation,

			Characteristics and symbols,
23.	7/6/2021	10.30AM-11.30AM	CMOS. Silicon Controlled Rectifier(SCR)-Two Transistor Model,
24.	9/6/2021	12.30PM-1.30PM	Switching Action, Characteristics, Phase Control application
25.	11/6/2021	12.30PM-1.30PM	Problems
MODULE-3 : OPERATIONAL AMPLIFIERS AND APPLICATIONS			
26.	12/6/2021	12.30PM-1.30PM	Introduction to Op-Amp
27.	14/6/2021	10.30AM-11.30AM	Op-Amp Input Modes
28.	16/6/2021	12.30PM-1.30PM	Op-Amp Parameters-CMRR
29.	18/6/2021	3.30PM-4.30PM	Input Offset Voltage and Current
30.	19/6/2021	12.30PM-1.30PM	Input Bias Current Input and Output Impedance,
31.	21/6/2021	10.30AM-11.30AM	Slew Rate, Application of Op-Amp Inverting Amplifier.
32.	9/7/2021	3.30PM-4.30PM	Non-Inverting Amplifier
33.	10/7/2021	12.30PM-1.30PM	Summer, Voltage Follower
34.	12/7/2021	10.30AM-11.30AM	Integrator
35.	14/7/2021	12.30PM-1.30PM	Differentiator
36.	16/7/2021	3.30PM-4.30PM	Comparator
37.	17/7/2021	12.30PM-1.30PM	Problems
MODULE-4 : BJT APPLICATIONS, FEEDBACK AMPLIFIERS AND OSCILLATORS			
38.	12/8/2021	11.00AM-1.00PM	BJT as an Amplifier, BJT as a Switch
39.	17/8/2021	9.00AM-11.00AM	Transistor Switch Circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay.
40.	19/8/2021	11.00AM-1.00PM	Feedback Amplifiers-Principle, Properties
41.	24/8/2021	9.00AM-11.00AM	Advantages of Negative Feedback
42.	26/8/2021	11.00AM-1.00PM	Types of Feedback, Voltage series Feedback

43.	31/8/2021	9.00AM-11.00AM	Gain Stability with feedback
44.	6/9/2021	4.00PM-5.00PM	Oscillator-Barkhaunsen's Criteria for Oscillator,
45.	7/9/2021	2.30PM-3.30PM	RC Phase Shift Oscillator.
46.	8/9/2021	12.30PM-1.30PM	Wien Bridge Oscillator
47.	9/9/2021	11.00AM-12.00PM	IC -555 Timer
48.	13/9/2021	4.00PM-5.00PM	Astable Oscillator using IC-555
49.	14/9/2021	2.30PM-3.30PM	Monostable Oscillator using IC-555
50.	15/9/2021	12.30PM-1.30PM	Problems
MODULE-5 : DIGITAL ELECTORNICS FUNDAMENTALS			
51.	16/9/2021	11.00AM-12.00PM	Difference between Analog and Digital signals, Number system-Binary, Hexadecimal.
52.	16/9/2021	4.00PM-5.00PM	Conversion-Decimal to Binary, Hexadecimal to decimal
53.	20/9/2021	4.00PM-5.00PM	Conversion- Binary to Decimal, Decimal to Hexadecimal.
54.	21/9/2021	2.30PM-3.30PM	Boolean algebra. Basic and Universal Gates.
55.	22/9/2021	12.30PM-1.30PM	Half Adder and Full Adder.
56.	22/9/2021	4.00PM-5.00PM	Multiplexer, Decoder, SR Flip Flops.
57.	23/9/2021	11.00AM-12.00PM	JK Flip Flops, Shift Register, 3-Bit Ripple Counter
58.	24/9/2021	9.30AM-10.30AM	Basic Communication System
59.	24/9/2021	4.00PM-5.00PM	Principle of Operation of Mobile Phone
60.	27/9/2021	4.00PM-5.00PM	Problems

Teaching and Learning Tools: Laptop/Mobile,Whiteboard (Jamboard App)/PowerPoint presentation

Text Books:

1. D.P. Kothari, I.J. Nagarath, "Basic Electronics" 2nd edn. Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

Reference Books:

1. D.P. Kothari, I.J. Nagarath, "Basic Electronics" 1st edn. Mc Graw Hill, 2014.
2. **Boylestad Nashelsky, "Electronic Devices and Circuit Theory",** Pearson Education 9th edition, 2007/ 11th edition, 2011.
3. **David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 5th edition, 2008.**
4. **Muhammed H. Rashid, "Electronics Devices and Circuits", Cengage Learning, 2014.**

Digital Library/E-Resources:

- 192.168.8.8:80/ Academic Resources
- 192.168.8.8:80/ Non-Academic Resources
- 192.168.8.8/gd
- 192.168.8.8/gd
- 192.168.8.8/gd
- 192.168.8.4

Innovative Practices:

1. **Seminars**
2. **Power Point Presentation**
3. **Quiz**

Note: Planning of syllabus is done as per VTU curriculum

Staff Signature **HOD**

Rao Bahadur .Y. Mahabaleshwarappa Engineering College Bellary

Dept ECE	2020 - 2021	Title: Report on Syllabus Status

REPORT ON SYLLABUS STATUS

Semester	Branch	Subject	Section	Name of the Staff
2	ECE	Basic electronics IPELN24	B	ASHWINI.K

Sl.No	Date	Period	Topics Covered	Remarks
1	30/4/21	3.30 - 4.30 pm	Introduction, Module-5 :- No s/m	
2	01/5/21	12.30 - 1.30 pm	Conversions.	
3	5/5/21	12.30 - 1.30 pm	class adjusted to Santosh sir, Numbers s/m	
4	7/5/21	3.30 - 4.30 pm	Boolean Algebra: Laws, Rules, Theorems	
5	8/5/21	12.30 - 1.30 pm	De-morgan's theorem, logic gates, simplification of Boolean	
6	10/5/21	10.30 - 11.30 pm	Simplifications of Boolean eqn's, Adders: Half adder, Full adder	
7	12/5/21	12.30 - 1.30 pm	Realization of Boolean exp. using gates, full adder	
8.	14/5/21	3.30 - 4.30 Pm	Multiplexer, 2:1, 4:1, 8:1 Mux	
9.	15/5/21	12.30 - 1.30 pm	Decoders; 2:4, 3:8 decoder	
10.	17/5/21	10.30 - 11.30 pm	Combinational circuit, sequential ckt, Flip flops	
11	19/5/21	12.30 - 1.30 pm	Clocked SR flip flop, J-K flip flop	
12	21/5/21	3.30 - 4.30 pm	Master slave J-K Flip flop & shift registers	
13	22/5/21	12.30 - 1.30 pm	Counters, 3-bit ripple Counters, Basic Communication System	
14	24/5/21	10.30 - 12 PM	Principle & operation of mobile phone, GSM, cellular telephone unit, Subtraction using 2's Complement	
15	26/5/21	12.30 - 1.30 pm	Module-3 - op-amp, Defn, Ideal char, Practical char (taken for B&D Sec) Block diagram, Symbol, parameters	
16	28/5/21	3.30 - 4.30 pm	Op-amp parameters circuit, I/p offset V/g, I/p Bias current, I/p Impedance	
17	29/5/21	12.30 - 1.30 pm	I/p offset current, o/p Impedance, slew rate, Realistic op-amp, assumptions & Golden rules of op-amp	
18	31/5/21	10.30 - 11.30 pm	Ideal Non-Inverting amplifier, Inverting Summer	
19	2/6/21	12.30 - 1.30 pm	Non-Inverting Summer, Integrator	
20	4/6/21	3.30 - 4.30 pm	Differentiator, voltage follower, Comparator - Non Inv	
21	5/6/21	12.30 - 1.30 pm	Inverting Comparator, Problems.	
22	7/6/21	10.30 - 11.30 pm	Problems on opamps	
23	9/6/21	12.30 - 1.30 pm	Problems, ~~Subtractor & Codes~~	
24	11/6/21	12.30 - 1.45 pm	Subtractor - Case(i), Problems	
25	12/6/21	12.30 - 1.30 pm	Subtractor - Case(ii), Problems QP	
26	14/6/21	10.30 Am - 11.30 Am	Module-1:- P-N junction diode, forward Biasing Reverse Biasing	
27	16/6/21	12.30 Pm - 1.30 Pm	Half wave Rectifier	
28	18/6/21	8.30 Pm - 4.40 pm	Full Wave Rectifier	
29	19/6/21	12.30 Pm - 1.40 Pm	Bridge Rectifier	
30	21/6/21	10.30 - 11.30,	Equivalent ckt of diode, V-I characteristics : forward characteristics.	

Signature of Staff In-charge: ASHWINI.K
Name of the Staff

Signature of the Head of the Department

Rao Bahadur .Y. Mahabaleshwarappa Engineering College Bellary

Dept: ECE	2020 - 2021	Title: Report on Syllabus Status

REPORT ON SYLLABUS STATUS

Semester	Branch	Subject	Section	Name of the Staff
2	ECE	Basic electronics 18ELN24	B	ASHWINI.K

Sl.No	Date	Period	Topics Covered	Remarks
31	9/7/21	3.30pm-4.30pm	1st IA Question Paper Problems solving	(Taken for B&D Section)
32	10/7/21	12.30pm-1.30pm	V-I characteristics: Forward & Reverse	
33	12/7/21	10.30pm-11.30pm	V-I characteristics for Si & Ge, Diode Parameters	Rpall
34	14/7/21	12.30pm-1.30pm	Breakdown mechanism of diode → Avalanche effect → Zener effect, V/g regulator	
35	16/7/21	3.30pm-4.30pm	Problems.	
36	17/7/21	12.30-1.30pm	Problems	
37	12/8/21	11-1pm	Zener diode :- Varying i/p V/g, Varying load	
38	17/8/21	9-11 Am	problems, Derivations of Half wave Rectifier.	
39	18/8/21	11-1 Pm	Derivations of Full-wave Rectifier	
40	24/8/21	9-11 Am	Problems	Rpall
41	26/8/21	11-1 Am	Bridge rectifiers	
42	31/8/21	9-11Am	Problems	
43	6/9/21	4-5Pm	Problems	
44	7/9/21	2.30-3.30	LED Photo coupler, Comparison b/w LED & I/R	
45	8/9/21	12.30-1.30	Fixed voltage regulations: (78XX Series) LM78XX series V/g regulator	
46	13/9/21	4-5Pm	Module 2 : JFET; Drain & Transfer characteristics	
47	14/9/21	2.30-3.30	Square law, MOSFET: Depletion & Enhancement	
48	16/9/21	12.30-1.30	SCR 2-transistor model, switching action	
49	16/9/21	11-12pm	Characteristics, Phase Control app, problems	
50	16/9/21	4-5Pm	BJT app's, f/b Amp & Oscillators, BJT-Amp	Rpall
51	20/9/21	4-5Pm	BJT as switch, Transistor switch circuit	
52	21/9/21	2.30-3.30	Feedback Amplifiers - Principal, Properties, advg of f/b	
53	22/9/21	4-5Pm	Types of feedback, V/g series f/b, Gain stability	
54	23/9/21	11-12 Pm	Oscillators - Barkhausen's Criteria for Oscillation	
55	24/9/21	9.30-10.30	RC phase shift, wein bridge oscillator	
56	24/9/21	4-5Pm	IC 555 Timer & Astable oscillator using IC 555	
57	27/9/21	4-5Pm	Problems	

Signature
Staff In-charge
ASHWINI.K
Name of the Staff

Signature
Head of the Department

COURSE EVALUATION AND ASSESSMENT SCHEME-2018

	What		To Whom	When/ Where (Frequency in the course)	Max Marks	Evidence Collected
Direct Assessment Methods	IA	Internal Assessment Tests	Students	Thrice(Average of three IA Tests)	30	Blue Books
		Assignment		Thrice(Before IA Test and average of 3 is taken)	10	Assignment Books
		Practical Assessment		Once	40	Practical evaluation
	FE	Final Examination		End of Course (Answering One of two questions from five Modules	100	Result sheet
		Practical Examination		One question from lot	100	Result sheet
Indirect Assessment Methods	Students Feedback		Students	End of the course	-	Questionnaire
	Course Exit Survey					

Questions for IA and FE will be designed to evaluate the various educational components (Bloom's taxonomy)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
ASSIGNMENT-I (2020-21Even Sem)

Staff Name: Ashwini K	**Sem/Sec: 2/B**	**Max Marks:10**
Course Name : Basic Electronics	**Course Code : 18ELN24**	

Q No	QUESTIONS	BTL	CO	PO
1	Translate the following: **i) $(125.75)_{10} = (?)_{16} = (?)_2$** **ii) $(11011.0110)_2 = (?)_{10} = (?)_{16}$.** **iii) $(8A.B8)_{16} = (?)_{10}$**	L2	4	1,2
2	Demonstrate the logic diagram using Basic Gates **B C + A B C + A B CD + A B C**	L2	4	1,2
3	Find $(111.11)_2$ - $(11011.11)_2$ using12's complement method.	L	4	1,2
4	Find the output expression for Inverting amplifier.	L1	2	1,2
5	Explain Full adder using two half adders	L2	2	1,2
6	Define Multiplexer? Explain48:1 Multiplexer	L1, L2	4	1,2
7	Explain the following parameters with respect to an op-amp **i) CMRR** ii) **Input impedance** iii) **Slew Rate** iv) **Input Offset Current** v) **Input Bias Current**.	L2	2	1,2
8	Define Binary Counter? Explain **3-bit** Ripple (asynchronous) Counter with Waveforms	L1, L2	4	1,2
9	Find the output expression for Inverting amplifier.	L1	2	1,2
10	Explain the working of a clocked JK Flip Flop, With a neat circuit diagram and truth table?	L2	4	1,2

Faculty Incharge

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CONTINUOUS INTERNAL EVALUATION -I (2020-21 EVEN Sem)

Staff Name: AK,VA,SM,SVP,PK	Sem /Sec:2nd/ A/B/C/D/E	Date: 7.07.2021 Time: 10 AM to 11.30AM
Course Name: Basic Electronics	Course Code: 18ELN24	Total Contact Hours:50
Max marks:30	Prerequisites: Fundamentals of Physics, Mathematics	

NOTE: ANSWER ANY ONE QUESTION FROM EACH PART

Q.NO	QUESTIONS	Marks	BTL	CO	PO
PART A	1) State and prove **De-Morgan's Theorems** for 3 variables. **OR** 2) Explain the principle and operation of Mobile phone With GSM Block Diagram.	6	L2,L3	4	1,2
PART B	3) a) Solve and Construct the logic diagram using Basic Gates $A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\,\overline{C} + \overline{A}\,\overline{B}\,C$ b) $\overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y} + \overline{X}\,\overline{Y}\,\overline{Z} + X\,\overline{Y}$ **OR** 4) Design Full Adder using three variables and Implement using two Half Adders	6	L1,L2	4	1,2
PART C	5) **Convert the following:** i) $(1025.75)_{10} = (?)_{16} = (?)_2$ ii) $(1011011.0110)_2 = (?)_{10} = (?)_{16}$. iii) $(F8E.B8)_{16} = (?)_{10}$ **OR** 6) a) Define Multiplexer ? Explain 8:1 Multiplexer. b) Define Decoder? Explain 3:8 decoder	6	L1,L2	4	1,2
PART D	7) Explain the following parameters with respect to an op-amp i) **CMRR** ii) **Input impedance** iii) **Slew Rate** iv) **Input Offset Current** v) **Input Bias Current**. **OR** 8) Explain the Working of 4bit Shift Register and Shift the 1011 using block diagram Serial Input Parallel Output[SIPO] Shifters	6	L2	1,4	1,2
PART E	9) i) With a neat circuit diagram and truth table, Explain the working of a clocked SR Flip Flop. ii) Define Binary Counter? Explain **3-bit** Ripple (asynchronous) Counter with Waveforms. **OR** 10) Design an adder circuit using op-amp to obtain an output voltage of $Vo = 0.4V_1 + 4V_2 + V_3$ where V1, V2, V3 are input voltages.	6	L1,L2	4,1	1,2

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

Staff Signature

Internal ASSESSMENT TEST -1.

Scheme of Evaluation [2020-21. EVEN SEM]

Date: 7-July-2021

Q1. a) De-Morgan's Theorems for 3 Variables [6M]

LHS $\overline{ABC} = \bar{A} + \bar{B} + \bar{C}$ RHS.

Complement of Product of 3 variables is equal to the Sum of the complement of the Individual Variables.

A	B	C	ABC	$\overline{ABC}$	$\bar{A}$	$\bar{B}$	$\bar{C}$	$(\bar{A}+\bar{B}+\bar{C})$
0	0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0	1
0	1	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0	1
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	0	1	1
1	1	1	1	0 ✓	0	0	0	0 ✓

(OR)

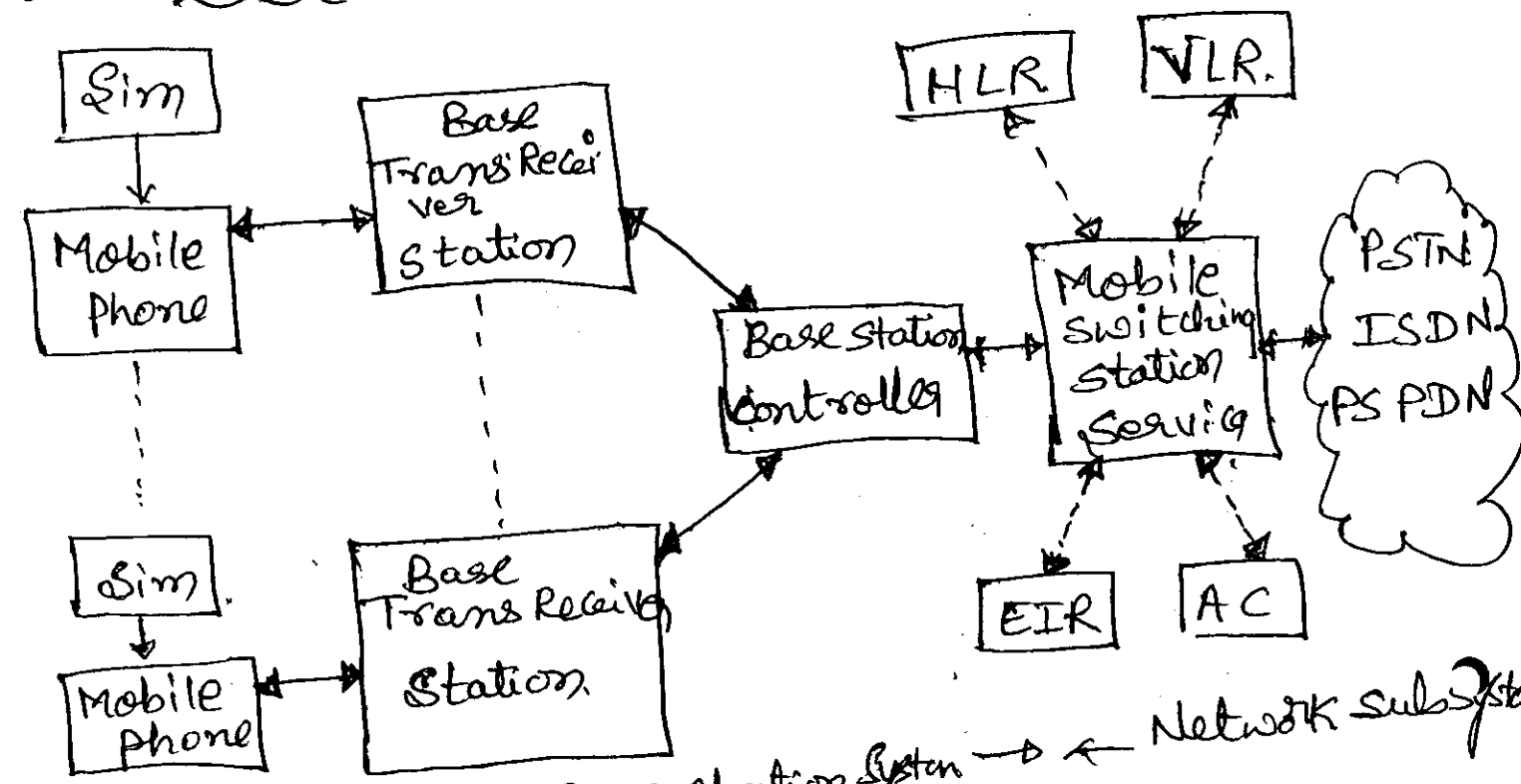
b) $\overline{(A+B+C)} = \bar{A}\,\bar{B}\,\bar{C}$ [6M] Any 1 They can Prove

LHS = RHS

Truth Table:

A	B	C	A+B+C	$\overline{(A+B+C)}$	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\bar{A}\,\bar{B}\,\bar{C}$
0	0	0	0	1	1	1	1	1
0	0	1	1	0	1	1	0	0
0	1	0	1	0	1	0	1	0
0	1	1	1	0	1	0	0	0
1	0	0	1	0	0	1	1	0
1	0	1	1	0	0	1	0	0
1	1	0	1	0	0	0	1	0
1	1	1	1	0 ✓	0	0	0	0 ✓

(2) Principle and operation of Mobile phone. [6M]



• 3M for diagram + 3M for explanation

5 Q $(1025.75)_{10} = (?)_{16} = (?)_2$

i) 16 | 1025
16 | 64 -1
4 -0

$0.75 \times 16 = 12.00 \rightarrow 12$ [C]
$00 \times 16 = 0.0 \rightarrow$

ii) $(1011011 \cdot 0110)_2 = (?)_{16}$

$(5 \quad B \cdot 6)_{16}$

$2^6\ 2^5\ 2^4\ 2^3\ 2^2\ 2^1\ 2^0 \quad 2^{-1}\ 2^{-2}\ 2^{-3}\ 2^{-4} = (?)_{10}$

$1\ 0\ 1\ 1\ 0\ 1\ 1 \cdot 0\ 1\ 1\ 0$

$1 \times 2^6 + 0 + 1 \times 2^4 + 1 \times 2^3 + 0 + 1 \times 2^1 + 1 \cdot 0 + 1 \times 2^{-2} + 1 \times 2^{-3} + 0$

$64 + 0 + 16 + 8 + 0 + 2 + 1 \cdot 0 + 0.25 + 0.125$

$(\quad)_b = (91.375)_{10}$

$(4\ 01 \cdot C)_{16} = (?)_b$

$0100\ 0000\ 0001 \cdot 1100)_2$

3) a) $Y = A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C$ [2+1=3M]

$= \bar{B}\bar{C}(A+\bar{A}) + \bar{A}B\bar{C} + \bar{A}\bar{B}C$ [$\because A+\bar{A}=1$]

$= \bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C$

$= \bar{B}[\bar{C} + \bar{A}C] + \bar{A}B\bar{C}$ [$\because \bar{C}+\bar{A}C = \bar{C}+\bar{A}$ →distrib]

$= \bar{B}(\bar{C}+\bar{A}) + \bar{A}B\bar{C}$

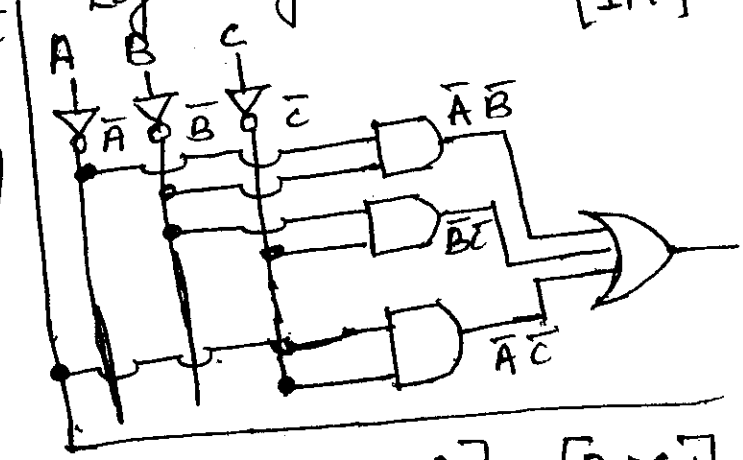
$= \bar{B}\bar{C} + \bar{B}\bar{A} + \bar{A}B\bar{C}$

$= \bar{B}\bar{C} + \bar{A}[\bar{B} + B\bar{C}]$

$= \bar{B}\bar{C} + \bar{A}(\bar{B}+\bar{C})$

$= \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C}$

Logic diagram [1M]



[3M]

b) $\bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y} + \bar{X}\bar{Y}\bar{Z} + X\bar{Y}$ [A+A=A]

$= \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y} + X\bar{Y}$

$= \bar{X}\bar{Y}[\bar{Z}+1] + X\bar{Y}$ [$\bar{A}+1=1$]

$= \bar{X}\bar{Y} + X\bar{Y}$ [$\bar{A}+A=1$]

$= \bar{Y}[\bar{X}+X]$

$= \bar{Y}$

4) Full Adder using 2 Half Adder

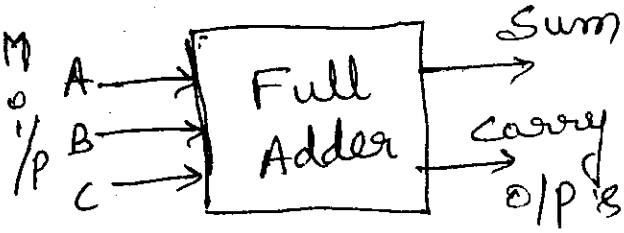
→ Full Adder is combinational logic ckt that performs the Arithmetic sum of 3 inputs bits & it consists of 2 outputs

6M = defination + schematic: 1M

= Truth Table : 1M

= Expression Reduction → 2M
Sum & carry

= Logic diagram → 2M



Truth Table

A	B	C	Sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

[1M]

Sum Expression : $\bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,\bar{C} + ABC$.

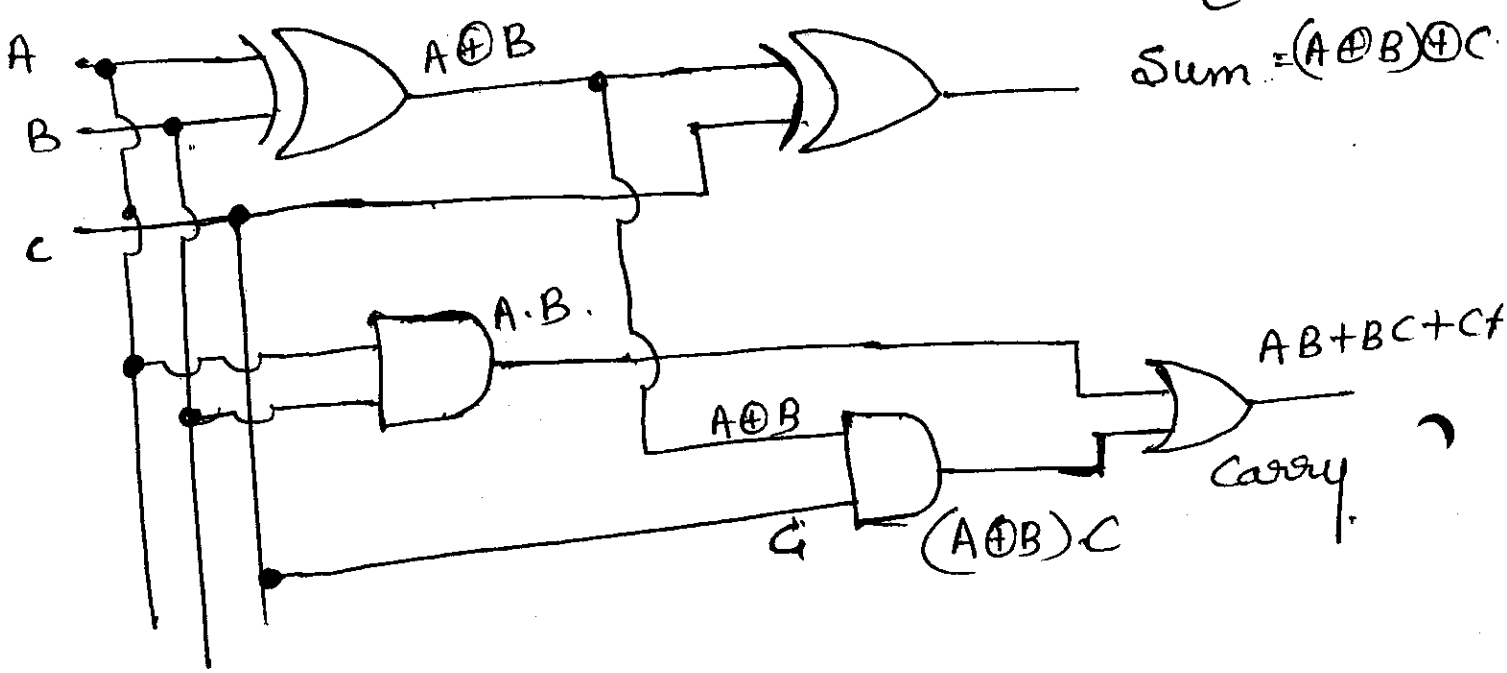
Reduce this Expression to → $(A \oplus B) \oplus C$. [1M]

$Sum = (A \oplus B) \oplus C$

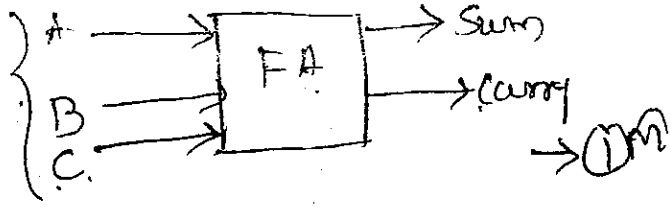
Carry Expression : $\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$. [1M]

Reduce this Expression carry : $AB + BC + CA$

[2M]



Full Adder Block diagram



→ (1M)

Sum : $C \oplus (A \oplus B)$.

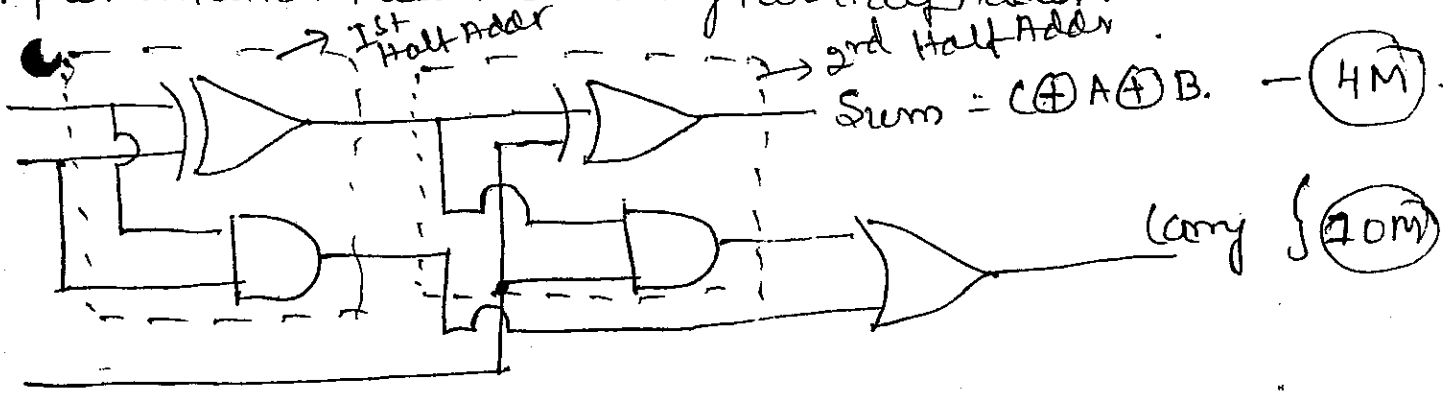
Carry : $C(A \oplus B) + AB$. } (3M)

working table

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

→ (2M)

Implementation Full Adder Using two Half Adder.



(4M)

(7om)

5) (i) ~~D-H~~ⁿ Conversion

(i) 16 | 1025

16 | 64 — 1

4 — 0.

Decimal part

$0.75 \times 16 \rightarrow 12.00 \rightarrow$

→ (1.2M).

$(0.75)_{10} = (0.C)$.

$1025 \rightarrow 401$.

$(1025.75)_{10} = (401.C)_{16}$ — (2M)

(6M)

$(401.C)_{16} = (0100\ 0000\ 0001.1100)_2$ → (2M).

(ii). $(1011011.0110)_2 = (91.375)_{10}$ — (2M)

$= (5B.6)_{16}$ → (2M).

(iii) $(F8E.B8)_{16} = (3982.71875)_{10}$ — (2M).

6) a) Defⁿ of MUX — 1M.

Block diagram of 8:1 MUX - 1M.

Working table — 1M.

Expression & logical Diagram → 2M

} 5M.

6. b) Defⁿ of Decoder → 1M.

Block diagram 3:8 Decoder - 1M.

working table → 1M.

Expression & logical Diagram - 2M

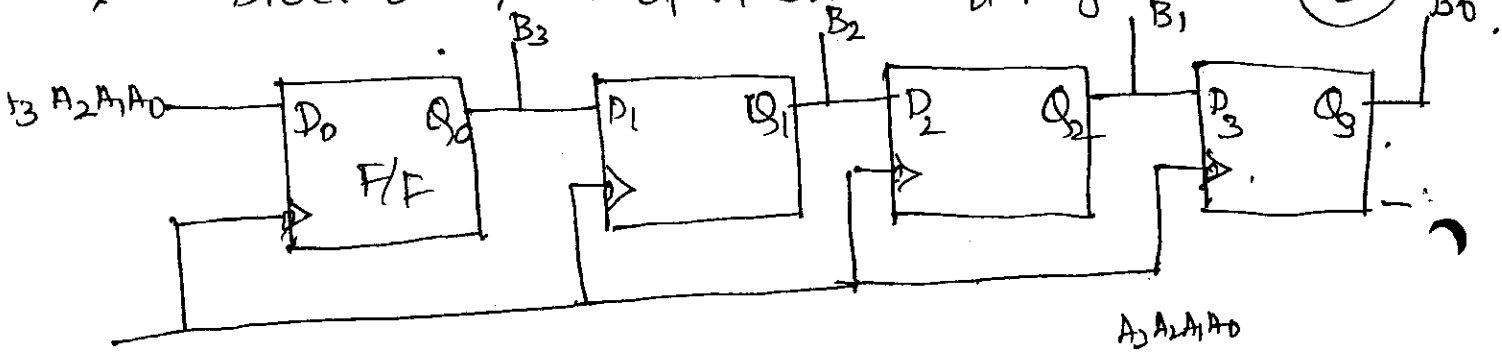
} 5M.

7. a) Each parameter defⁿ. carries - 1M = 5x1

Each parameter Expression with Unit - 1M = 5x1.

} 10M.

8 a) Block diagram of 4 bit Shift Register. — 2M



Clk	D	B_3	B_2	B_1	B_0
↓	A_0	A_0	0	0	0
↓	A_1	A_1	A_0	0	0
↓	A_2	A_2	A_1	A_0	0
↓	A_3	A_3	A_2	A_1	A_0
↓					

2M

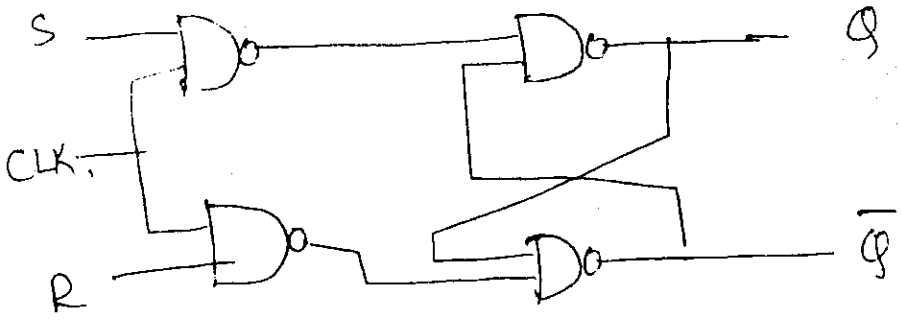
Ex: $A_3A_2A_1A_0$ = 1011

Clk	D	B_3	B_2	B_1	B_0
↓	1	1	0	0	0
↓	1	1	1	0	0
↓	0	0	1	1	0
↓	1	1	0	1	1
↓					

2M

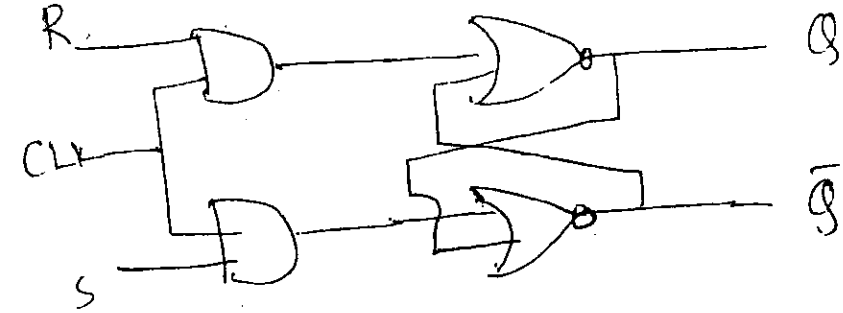
06M

(i). Clocked SR flip flop.



(4M)

(OR)



→ (2M)

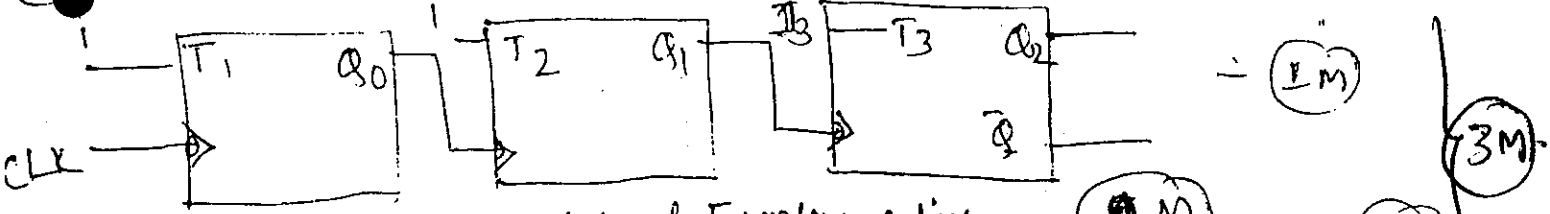
Truth table → (1M)

CLK	S	R	Q	$\bar{Q}$	Comments.
⌐_	0	0	Q	$\bar{Q}$	NC.
⌐_	0	1	0	1	Reset
⌐_	1	0	1	0	Set
⌐_	1	1	X	X	Invalid

Explanation of SR flip flop. → (2M).

3M

(ii). 3 bit Ripple Counter



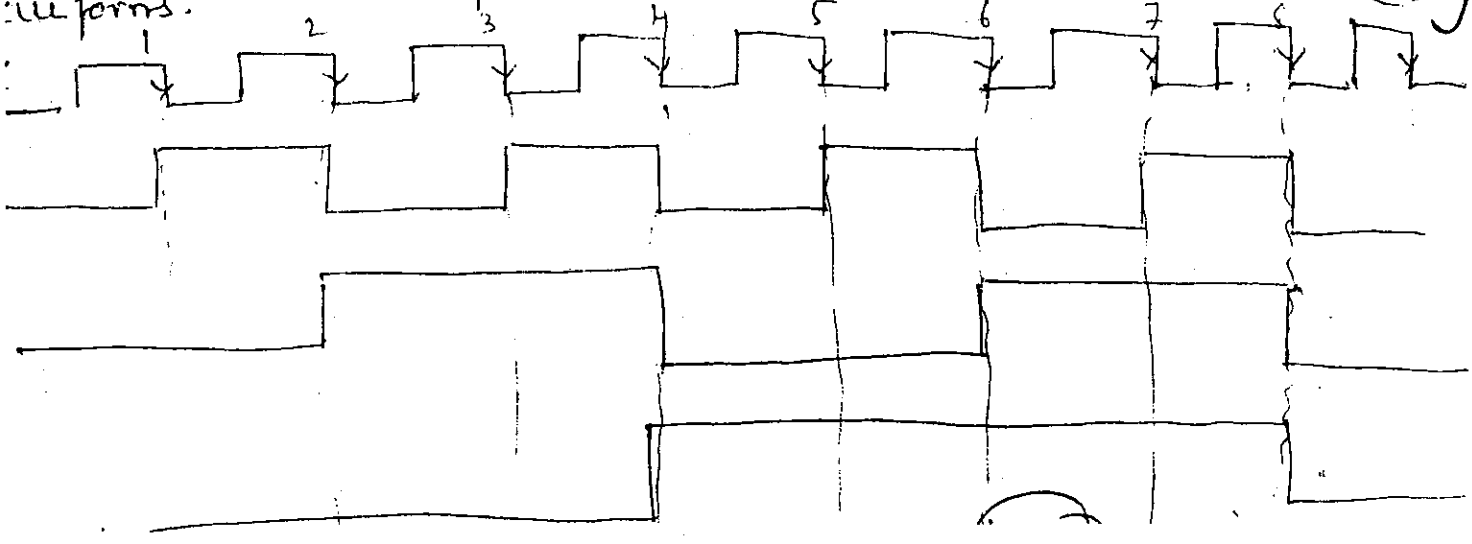
→ (1M)

3M.

Working table & Explanation — (2M).

→ (2M)

Waveforms.



10) Soln Given. $V_o = 0.4V_1 + 4V_2 + V_3$ — (1)

V_o where V_1, V_2 & V_3 are input.

W.K.T. $V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$ — (2)

Compare Eqn (1) & (2) in Eqn (1) having +ve sign hence, design. Inverting summer First, then Design Inverting Amplifire. with gain 1.

$\therefore V_{01} = -[0.4V_1 + 4V_2 + V_3]$ - (3)

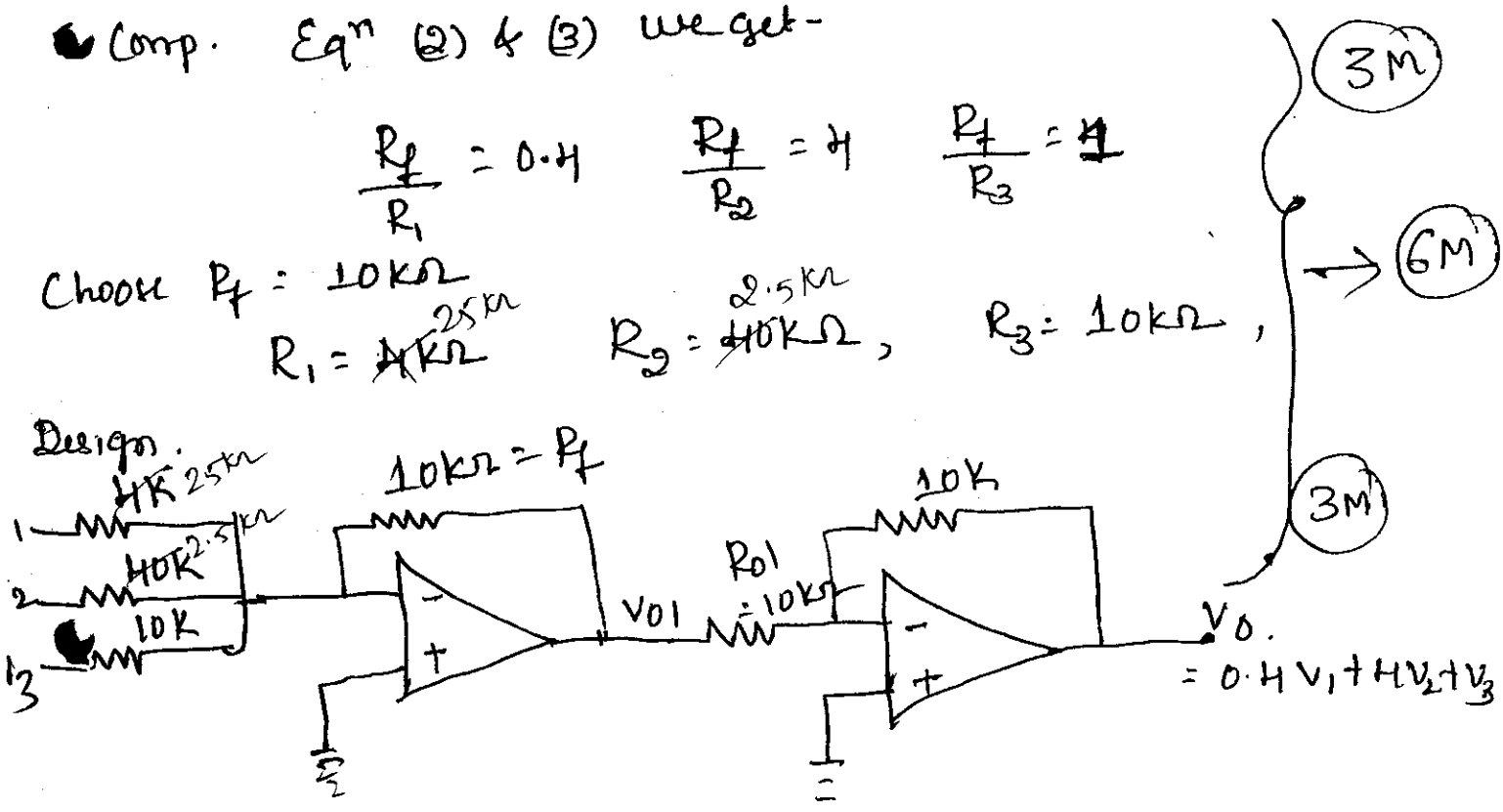
Comp. Eqn (2) & (3) we get-

$\frac{R_f}{R_1} = 0.4$ $\frac{R_f}{R_2} = 4$ $\frac{R_f}{R_3} = 1$

Choose $R_f = 10K\Omega$

$R_1 = 25K\Omega$ $R_2 = 2.5K\Omega$, $R_3 = 10K\Omega$,

Design.



Kelin Prashanth
Staff Signature

I A Co-ordinater

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IA-1 PERFORMANCE ANALYSIS

SUB: Basic Electronics AY: 2020-21 (EVEN)

Course Code: 18ELN24 Sem/Sec: 2B

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
Co Mapping	CO4	CO4	CO4	CO4	CO4	CO4	CO1	CO4	CO4	CO1
Max Marks for questions	6	6	6	6	6	6	6	6	6	6
Marks scored	244	18	39	198	74	158	236	29	79	81
no of students Attempted	47	49	49	46	48	47	47	49	49	46
60% of Max Marks for questions	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
no of students scored > 60% of marks/Question	39	4	7	37	12	29	41	6	13	2
Average no of students >60% of marks/Question	0.8298	0.0816	0.1429	0.80435	0.25	0.617	0.8723	0.1224	0.2653	0.0435
Percentage	83%	80%	14%	80%	25%	62%	87%	12%	27%	4%

Marks range	0-20	20 to 30
No. of Students	14	36

Staff Incharge
(MRS. ASHWINI. K)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

ASSIGNMENT-II (2020-21 Even Sem)

Staff Name: Ashwini K	**Sem/Sec: 2/B**	**Max Marks:10**
Course Name : Basic Electronics	**Course Code : 18ELN24**	

Q No	QUESTIONS	BTL	CO	PO
1	Explain the operation of p-n junction diode under forward and reverse biased condition& Draw V-I characteristics of diode.	L1	1	1,2
2	Define Zener diode? With neat circuit diagram, explain the operation of a voltage regulator with varying input conditions (Line regulation).	L1	1	1,2
3	A diode circuit shown below has E=1.5 V, RI=10 Ω assume V_F=0.7 V. Find I_F for i) rd=0 ii) rd=0.25Ω	L1	1	1,2
4	Explain the working of Half wave rectifier, with a neat circuit diagram and waveform, and derive the expression for Efficiency and ripple factor.	L1	1	1,2
5	In a full wave rectifier uses 2 diodes having internal resistance of 20 Ω each. The transformer RMS secondary voltage from center to each end is 50 V. Find **I_m, I_{DC}, I_{RMS}, Vdc, efficiency** and **ripple factor.** Formulate the output expression for Inverting amplifier.	L1	1	1,2
6	A silicon diode has Is =10nA operating at 25° C. Find diode current if the forward bias voltage is 0.6 V. Assume $\eta = 2$.	L1	1	1,2
7	Explain Comparators with mathematical analysis and waveforms	L1	2	1,2
8	How op-amp acts as Integrator and voltage follower.	L1	2	1,2
9	Extend the output expression for non inverting Summer with circuit diagram.	L2	2	1,2
10	Develop an adder circuit for the output voltage V_0= - (2V1 + $3V_2$ + $5V_3$).	L3	2	1,2

Faculty Incharge

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CONTINUOUS INTERNAL EVALUATION (CIE) -II (2020-21 EVEN Sem)

Staff Name: VA, PK, SVP, AK, SM	**Sem / Sec: 2nd / A/B/C/D/E**	**Date: 17/09/2021** Time: 3.30PM to 05.00PM
Course Name: Basic Electronics	**Course Code:18ELN24**	**Total Contact Hours: 50**
Max marks: 30	**Prerequisites: Fundamentals of Physics, Mathematics**	

NOTE: ANSWER ANY ONE QUESTION FROM EACH PART

Q.NO	QUESTIONS	Marks	BTL	CO	PO
PART A	1) Outline the circuit and Derive the equation for a) Differentiator b) Comparator. OR 2) Outline the circuit and Derive the equation for a) Integrator b) Voltage follower	6	L2	1, 2	1,2
PART B	3) Explain the operation of Photodiode and LED? **OR** 4) Explain HWR with capacitor filter & Waveforms?	6	L2	1, 2	1,2
PART C	5) Outline an inverting amplifier using an op-amp and derive expression for its output voltage. **OR** 6) Outline a Non- inverting amplifier using an op-amp and derive expression for its output voltage.	6	L2	1, 2	1,2
PART D	7) Explain the operation of PN Junction Diode under forward and reverse biased condition. **OR** 8) Explain FWR with Circuit Diagram and Waveforms	6	L2	1, 2	1,2
PART E	9) A Half Wave Rectifier is supplied from 230V-50Hz, Supplied with step-down ratio is 3:1 to a load of 10KΩ, the forward resistance is 75Ω and secondary resistance is 10Ω. Find Average DC Current, RMS Value of a Current, DC Output Voltage, Efficiency & Ripple Factor **OR** 10) Find the average voltage, rectification efficiency and ripple factor in a full wave rectifier, if the input is from a 30-0-30V transform. The load and diode forward resistance are 100Ω and 10Ω respectively.	6	L1	1,2	1,2

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

Kevanamar

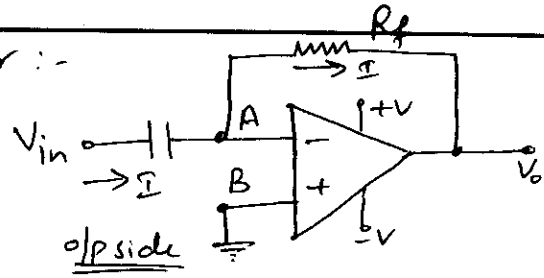
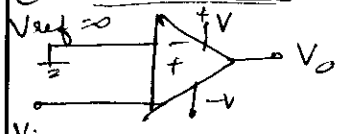
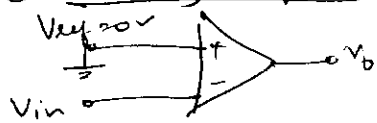
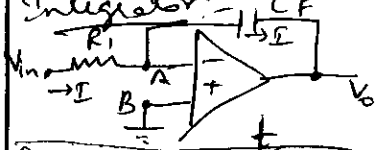
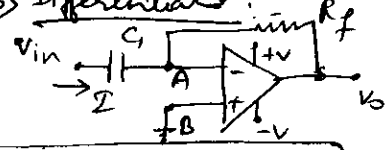
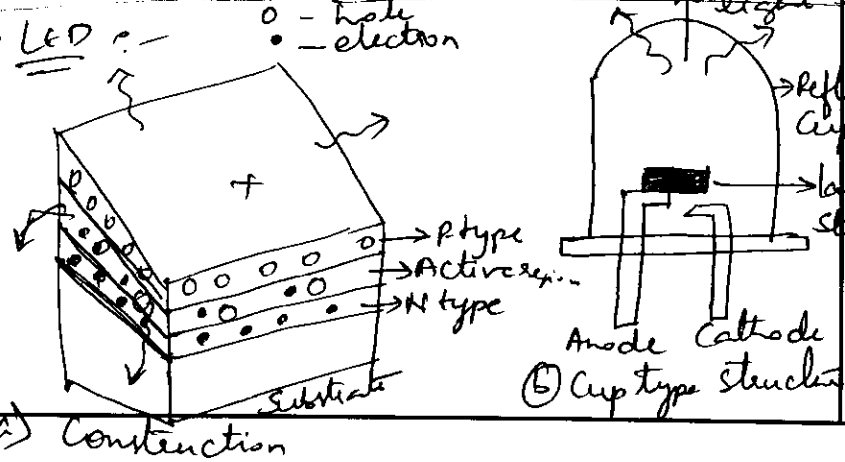
Staff Signature

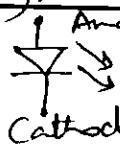
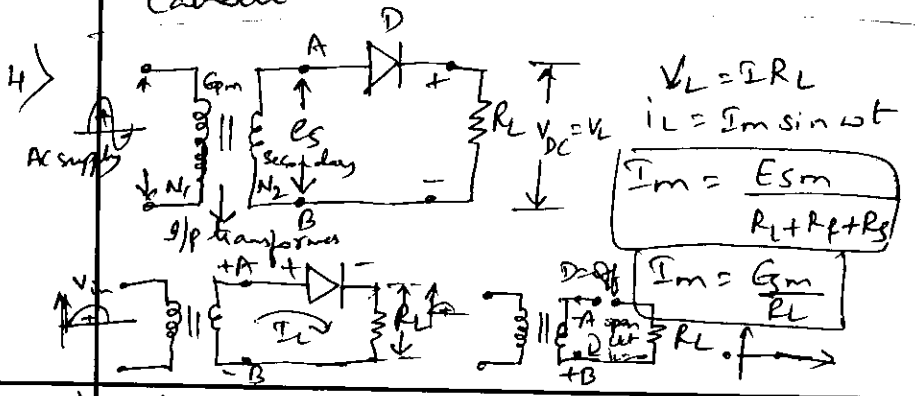
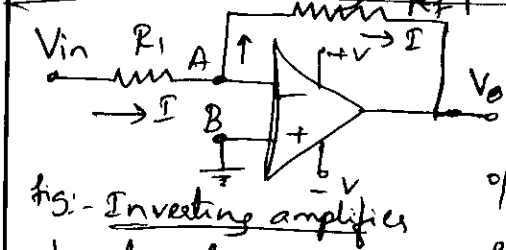
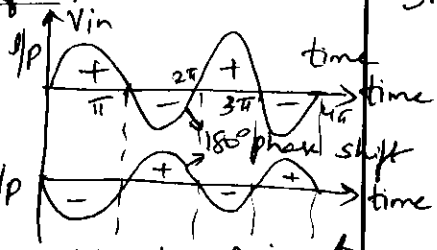
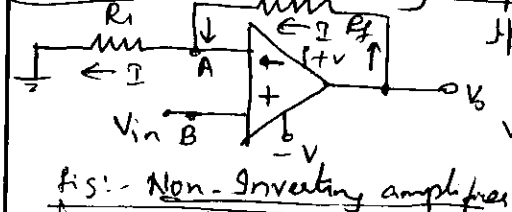
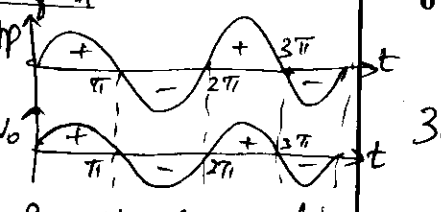
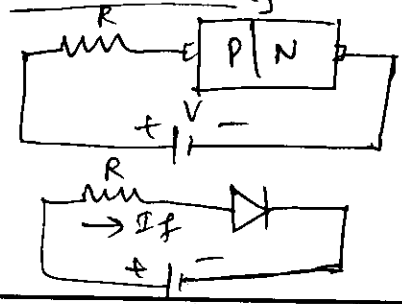
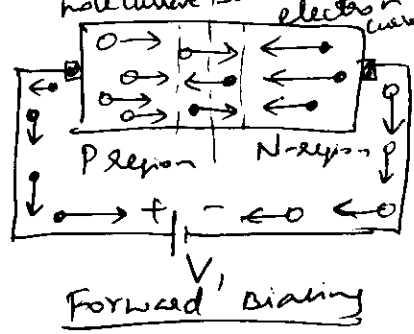
RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

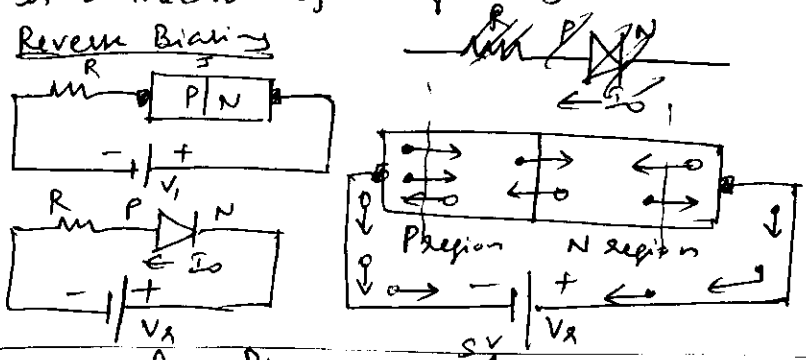
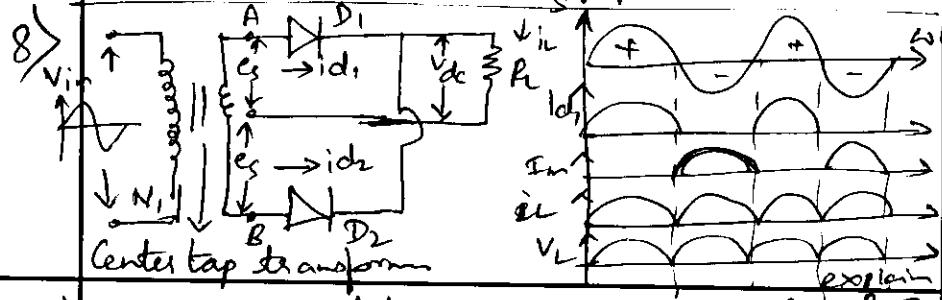
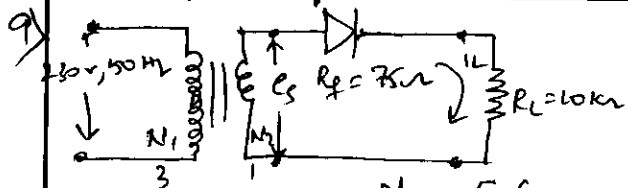
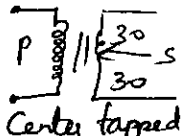
SCHEME OF EVALUATION -II (2020-21 EVEN Sem)

Staff Name: VA, PK, SVP, AK, SM	Sem / Sec: 2nd / A/B/C/D/E	Date: 17/09/2021 Time: 3.30PM to 05.00PM
Course Name: Basic Electronics	Course Code:18ELN24	Total Contact Hours: 50
Max marks: 30	Prerequisites: Fundamentals of Physics, Mathematics	

NOTE: ANSWER ANY ONE QUESTION FROM EACH PART

Q.NO	QUESTIONS	Marks	BTL	CO	PO
PART A 1)	a) Differentiator :-  from V_{GC} $V_A = V_B = 0$ I/P side $I = C_1 \frac{d}{dt}(V_{in} - V_A)$ $I = C_1 \frac{d}{dt} V_{in} \rightarrow (1)$ o/p side $I = \frac{V_A - V_o}{R_f} = -\frac{V_o}{R_f} \rightarrow (2)$ At node A: Apply KVL, $\therefore$ Eqn (1) = (2) $V_o = -R_f C_1 \frac{dV_{in}}{dt}$	3m 3m			
	b) Comparator :- ① Non-Inverting  i) $V_{in} > V_{ref}$ $V_o = +V_{sat}$ $V_o = +V_{sat} = +V$ ii) $V_{in} < V_{ref}$ $V_o = -V_{sat} = -V$ ② Inverting comparator  $V_{in} > V_{ref}$ $V_o = -V_{sat} = -V$ $V_{in} < V_{ref}$ $V_o = +V_{sat} = +V$	6 3m 3m	L2	1, 2	1,2
	2a) Integrator :-  $V_o = -\frac{1}{R_1 C_f} \int_0^t V_{in}\, dt$ 2b) Differentiator :-  $V_o = -R_f C_1 \frac{d}{dt} V_{in}$	3m 3m			
PART B 2)	LED :-  a) Construction b) Cup type structure	6 3m	L2	1, 2	1,2

	⑥ Symbol  Explanation  $V_L = IR_L$ $i_L = I_m \sin\omega t$ $I_m = \frac{E_{sm}}{R_L+R_f+R_s}$ $I_m = \frac{G_m}{R_L}$	3m 3m 3m			
PART C	5) Ideal Inverting Amplifier  fig:- Inverting amplifier  fig:- waveform of inverting amplifier	3m	L2	1, 2	1,2
	i/p side: from $V_A = V_B = 0 \rightarrow ①$ $I = \frac{V_{in}-V_A}{R_1} = \frac{V_{in}}{R_1}$ $I = \frac{V_{in}}{R_1} \rightarrow ②$ From o/p side $I = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$, $I = \frac{-V_o}{R_f} \rightarrow ③$	KCL at node A $\frac{V_{in}}{R_1} = \frac{-V_o}{R_f}$ $\frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$ $V_o = -\frac{R_f}{R_1} V_{in}$	3m			
	Ideal Non-Inverting amplifier  fig:- Non-Inverting amplifier  fig:- Non-Inv amplifier	6 3m			
	$V_A = V_B = V_{in} \rightarrow ①$ From i/p side $I = \frac{V_A - 0}{R_1}$ $I = \frac{V_{in}}{R_1} \rightarrow ②$ From o/p side $I = \frac{V_o - V_A}{R_f}$ $I = \frac{V_o - V_{in}}{R_f} \rightarrow ③$ Current entering = Current leaving $\frac{V_{in}}{R_1} = \frac{V_o - V_{in}}{R_f}$, $\frac{V_{in}}{R_1} = \frac{V_o}{R_f} - \frac{V_{in}}{R_f}$	$\frac{V_{in}}{R_1} + \frac{V_{in}}{R_f} = \frac{V_o}{R_f}$ $\frac{V_o}{R_f} = V_{in}\left[\frac{1}{R_1} + \frac{1}{R_f}\right]$ $A_V = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$ $V_o = \left(1 + \frac{R_f}{R_1}\right) V_{in}$	3m			
PART D	⑦ forward Bias  V  Forward biasing	3m 6	L2	1, 2	1,2

	External d.c V/g Connected in such a way that P region is connected to P & n region is connected negative of dc V/s → Forward Biasing Reverse Biasing  8)  	3m 3m 3m			
PART E	9)  Given: R_f=7Ω, R_L=10kΩ, R_s=10Ω $\therefore E_{p(rms)} = 230$, $\frac{N_2}{N_1} = \frac{E_{s(rms)}}{E_{p(rms)}}$, $E_{s(rms)} = \frac{E_{p(rms)} N_2}{N_1}$ $= \frac{230 \times 1}{3}$ $E_{sm} = \sqrt{2}\, E_{s(rms)} = \sqrt{2}(76.667)$ $E_{sm} = 108.423$ V $E_{s(rms)} = 76.667$ V ① $I_m = 10.75$ mA ② $I_{dc} = 3.422$ mA ③ $I_{rms} = \frac{I_m}{2} = 5.375$ mA ④ $V_{dc} = 34.22$ V $P_{dc} = 0.1171$ W $P_{AC} = 0.2913$ W ⑤ $\eta = 40.19\%$ ⑥ $\gamma = 1.21$ 10) Transformer 30-0-30 V $E_{s(rms)} = 30$ V $E_s = \sqrt{2}\, E_{s(rms)} = \sqrt{2} \times 30$ $E_s = 42.426$ V $I_m = 0.3856$ A $I_{dc} = 0.2455$ A $V_{dc} = V_{av} = I_{dc} R_L = 24.55$ V efficiency $\eta = \frac{P_{dc}}{P_{AC}} \times 100$ % $\eta = \frac{6.027}{8.177} \times 100$ $P_{dc} = 6.027$ W $\eta = 73.69\%$ $P_{AC} = 8.1778$ W $\gamma = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}} = 0.48 = \gamma$  	3m 3m 3m 3m	6	L1	1,2	1,2

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

Staff Signature

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IA-2 PERFORMANCE ANALYSIS

SUB: Basic Electronics — AY: 2020-21 (EVEN)

Course Code: 18ELN24 — Sem/Sec: 2B

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
Co Mapping	CO1	CO2	CO1	CO2	CO1	CO2	CO1	CO2	CO1	CO2
Max Marks for questions	6	6	6	6	6	6	6	6	6	6
Marks scored	126	172	150	148	150	147	108	186	264	28
no of students Attempted	49	50	49	50	49	50	49	50	49	50
60% of Max Marks for questions	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
no of students scored > 60% of marks/Question	21	29	25	25	25	25	18	31	44	5
Average no of students >60% of marks/Question	0.4286	0.58	0.5102	0.5	0.5102	0.5	0.3673	0.62	0.898	0.1
Percentage	43%	58%	51%	50%	51%	50%	37%	62%	90%	10%

Marks range	0-20	20 to 30
No. of Students	0	50

Staff Incharge
(Mrs. ASHWINI.K)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
ASSIGNMENT-III (2020-21 Even Sem)

Staff Name: Ashwini K	**Sem/Sec: 2/B**	**Max Marks:10**
Course Name : Basic Electronics	**Course Code : 18ELN24**	

Q. No	QUESTIONS	BTL	CO	PO
1	Explain how transistor can be used as an amplifier.	L2	2	1,2
2	Explain how the transistor used to Switch an LED ON/OFF, with the neat circuit diagram and give the necessary equations.	L	2	1,2
3	Explain the operation of IC-555 timer as an astable Oscillator with neat circuit diagram and necessary equations	L2	1	1,2
4	Define Oscillator .Explain the Barkhaunsen's conditions for oscillations with relevant sketch and equations	L1, L2	3	1,2
5	Explain the operation of an RC phase shift oscillator with relevant equations.	L2	3	1,2
6	Find its frequency of oscillations, Solve for RC phase shift oscillator using R=100 kΩ & C=10nF.	L1	3	1,2
7	Explain the voltage series feedback circuit and derive an equation for voltage gain with feedback	L2	3	1,2
8	Explain the two transistor model of SCR	L2	1	1,2
9	Explain the construction and operation of **p-channel E-MOSFET** with their drain and transfer characteristics	L2	1	1,2
10	Explain the construction and operation of **p-channel JFET** with their drain and transfer characteristics.	L2	1	1,2

Faculty Incharge

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CONTINUOUS INTERNAL EVALUATION (CIE)-III (2020-21 EVENSem)

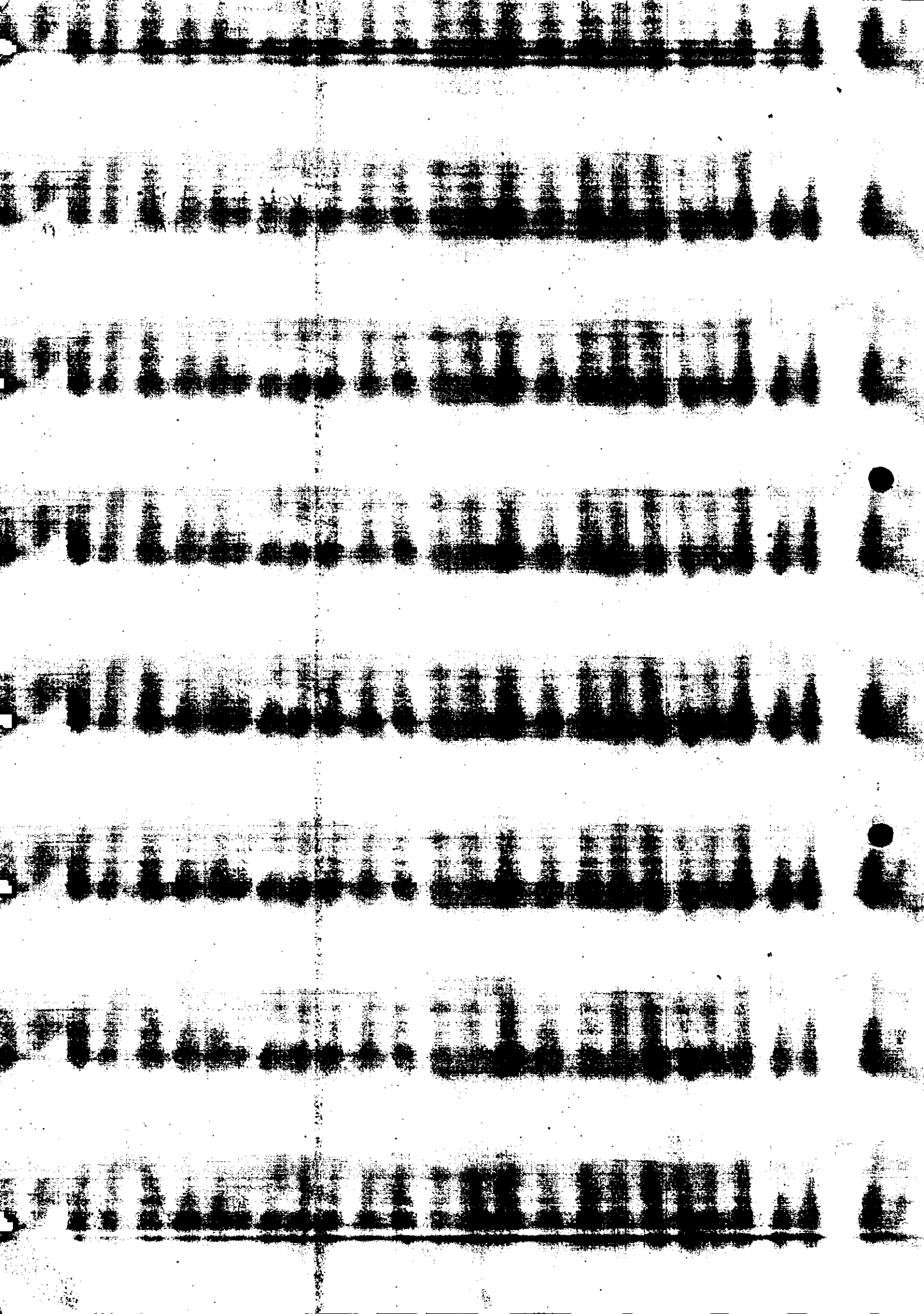
Staff Name: (VA, PK, SVP, AK, SM)	Sem /Sec: 2nd/ A/B/C/D/E	Date: 22/9/21 Time: 3.30PM to 05.00PM
Course Name: Basic Electronics	Course Code:18ELN24	Total Contact Hours: 50
Max marks: 30	Prerequisites:Fundamentals of Physics,Mathematics	

NOTE: ANSWER ANY ONE QUESTION FROM EACH PART

Q.NO	QUESTIONS	Marks	BTL	CO	PO
PART A	1) Explain how the transistor used to Switch an LED ON/OFF and give the necessary equations With the neat circuit diagram OR 2) Explain how transistor is used as Voltage amplifier.	6	L2	2	1,2
PART B	3) Explain the operation of IC-555 timer as an astable Oscillator with neat circuit diagram and necessary equations OR 4) Define Oscillator .Explain the Barkhaunsen's conditions for oscillations with relevant sketch and equations.	6	L1,L2	3	1,2
PART C	5) Explain the operation of an RC phase shift oscillator with relevant equations OR 6) Explain the voltage series feedback circuit and derive an equation for voltage gain with feedback.	6	L2	3	1,2
PART D	7)Explain the construction and operation of N-channel JFET With their drain and transfer characteristics. OR 8) Explain the construction and operation of N-channel E-MOSFET with their drain and transfer characteristics.	6	L2	1	1,2
PART E	9)Explain the two transistor model of SCR and also explain V-I characteristics of SCR. 10) i) Determine for RC phase shift oscillator using R=10 k.Q & C=1nF. Find its frequency of oscillations. Ii) what should be value of C for astable frequency of 300KHz, R1=R2=7.5K ohm	6	L2, ~~L3~~	2	1,2

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

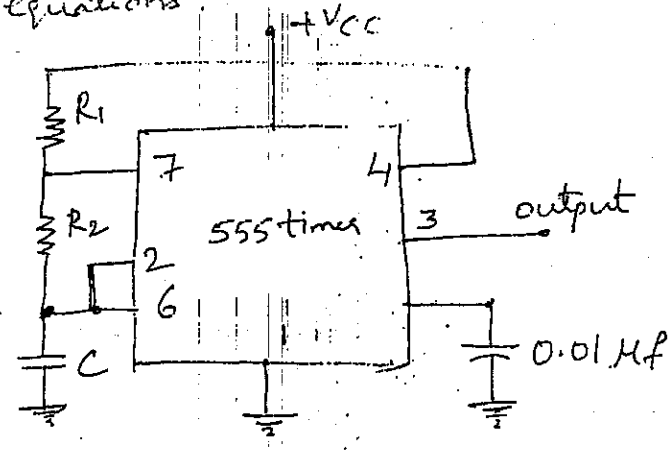
Staff Signature

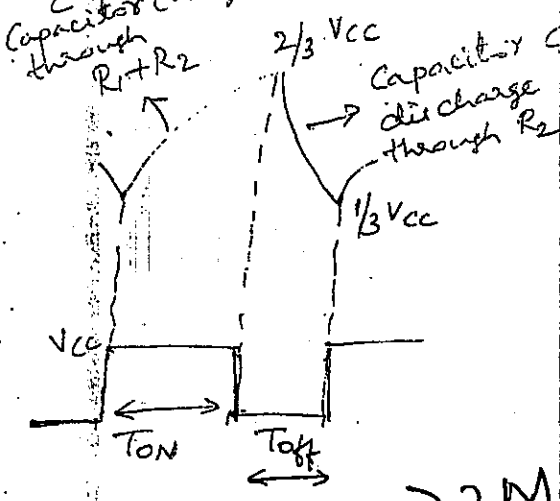


Part B

3) Explain the operation of IC-555 timer as an astable oscillator with neat circuit diagram & necessary equations.

Solu:





→ 2M

fig:- Astable operation using 555 IC

$T_{high} \approx 0.7 (R_1 + R_2) C$: Beyond 2/3 V_{CC} : charging

$T_{low} \approx 0.7 R_2 C$: Below 1/3 V_{CC} : discharging

oscillation period : $T = T_{high} + T_{low}$

oscillation frequency : $f = \frac{1}{T} = \frac{1}{T_{high} + T_{low}}$

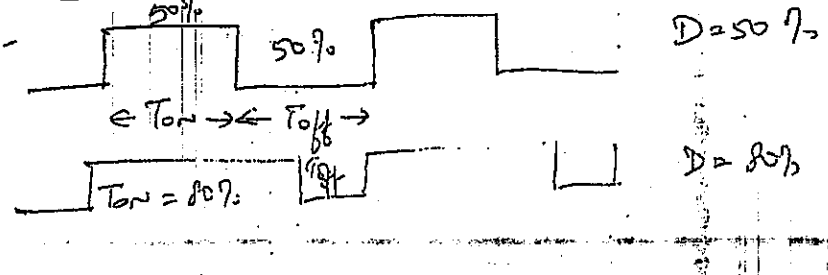
$$f = \frac{1}{0.7(R_1+R_2)C + 0.7R_2C} = \frac{1}{0.7(R_1C + R_2 2C)} = \frac{1.44}{[R_1 + R_2(2)]C}$$

$$\boxed{f = \frac{1.44}{(R_1 + 2R_2)C}} \text{ Hz}$$

Duty cycle : $D = \frac{T_{high}}{T_{high} + T_{low}} = \frac{R_1 + R_2}{R_1 + 2R_2}$ → 2M

$$\boxed{D = \frac{R_1 + R_2}{R_1 + 2R_2}}$$: less than 50%

Ex:-



Explanation ——→ 2 M

Scheme of Evaluation CIE-III (~~2020-21~~) Even

Course Name : Basic Electronics

Course Code : 18ELN24

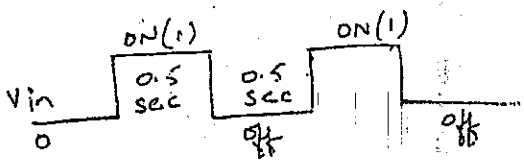
Max Marks : 30

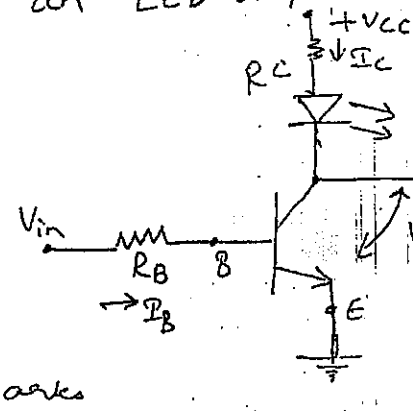
Sem/sec : 2nd / A/B/C/D/E

Part - A

1) With the neat circuit diagram explain how the transistor used to switch an LED ON/OFF and give the necessary equations.

Sol





→ 3M

Explanation → 4 marks

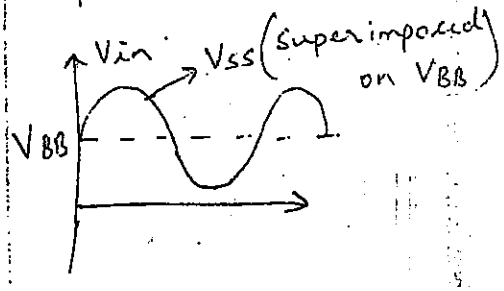
LED is ON for 0.5 sec [Vin = 1]

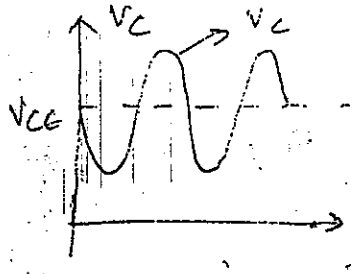
& LED is off for 0.5 sec [Vin = 0] → 1 mark

→ 3M

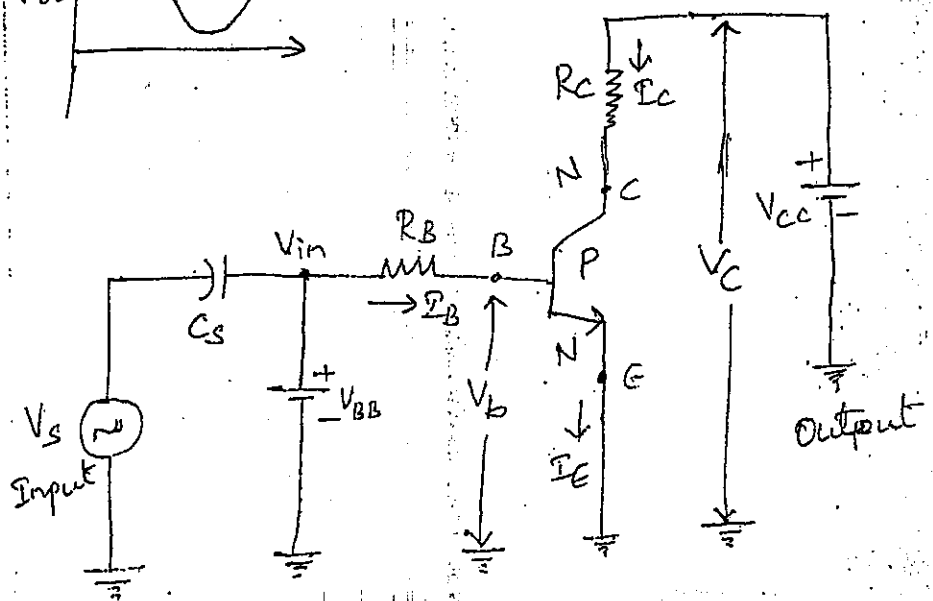
2) Explain how transistor is used as voltage amplifier.

Sol





3M



Explanation →

Derivation upto $\left[A_v = \frac{R_c}{r_o'}\right]$ → 3M

4) Define oscillator. Explain the Barkhausen's conditions for oscillations with relevant sketch and equations.

Definition of oscillator → 1M

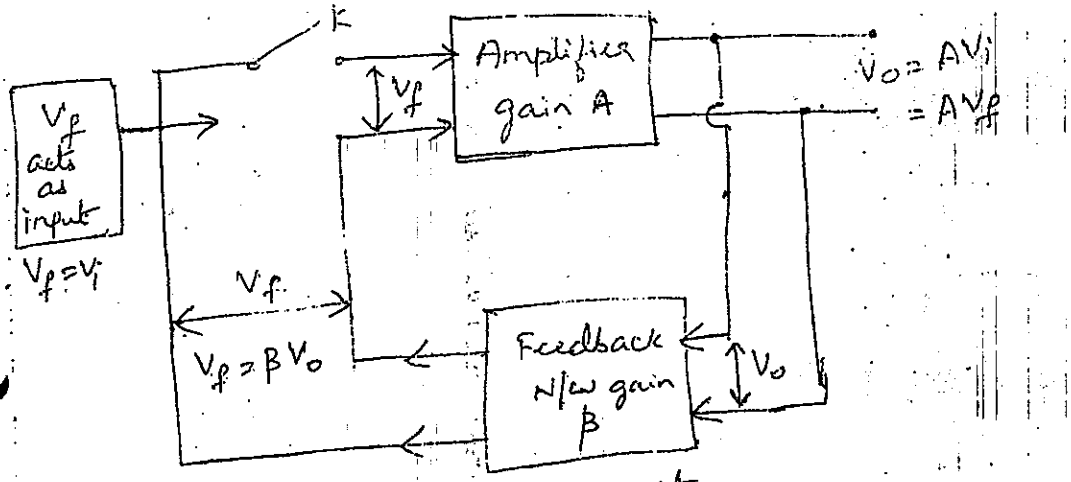


fig: Basic oscillator circuit

$$A_F = \frac{V_o}{V_{in}} = \frac{A}{1+A\beta}$$

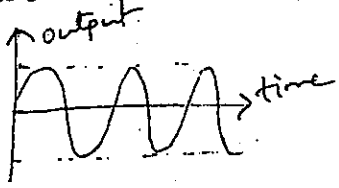
When $V_{in} = 0$, gain $A_F \to \infty$ and

$1 + A\beta = 0$, $\boxed{A\beta = -1}$ i.e., $\boxed{A\beta = -1 + j0 = 1\angle +180^\circ}$

under this condition $V_i = 0$ & V_f drives the circuit into oscillations.

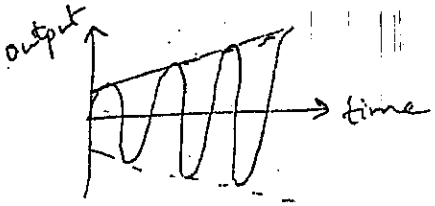
→ The condition $\boxed{A\beta = -1}$ is called Barkhausen criteria for oscillations

3M

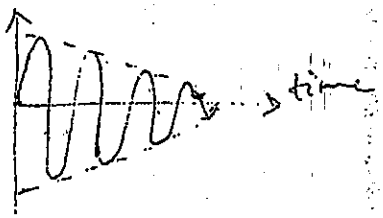


$|A\beta| = 1$ (0° or 360°)
undamped (sustained oscillations)

3M



$|A\beta| > 1$
Increasing amplitude (damped oscillations)



$|A\beta| < 1$
Decreasing amplitude (damped oscillations)

Explanation → 1M

1M

Part - C

5) Explain the operation of an RC phase shift oscillator with relevant equations.

Soln

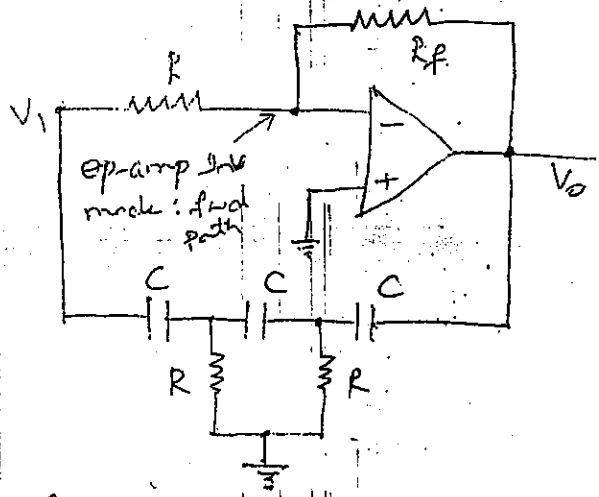


fig: RC phase shift oscillator

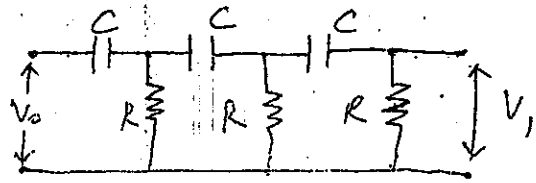
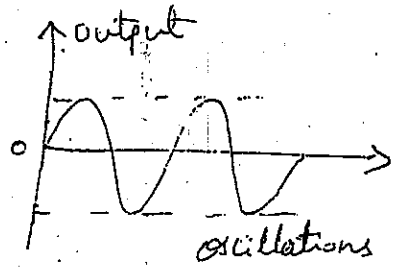


fig:- RC Phase shifting N/w



→ 3M

→ frequency of oscillations given by

$$f_o = \frac{1}{RC\sqrt{6}} \quad \text{i.e.,} \quad f_o = \frac{1}{2\pi RC\sqrt{6}}$$

; $|\beta| = \frac{1}{29}$ & feedback path introduces 180° phase shift

→ To satisfy Barkhausen condition, $|A\beta| = 1$

i.e., $|A| = \frac{1}{|\beta|} = 29$

→ for inverting amplifier using op-amp. The gain is $|A| = \frac{R_f}{R} = 29$

$\therefore$ $R_f \geq 29R$

→ 3M

Explanation → 1M

---

6) Explain the voltage series feedback circuit and derive an equation for voltage gain with feedback.

Soln

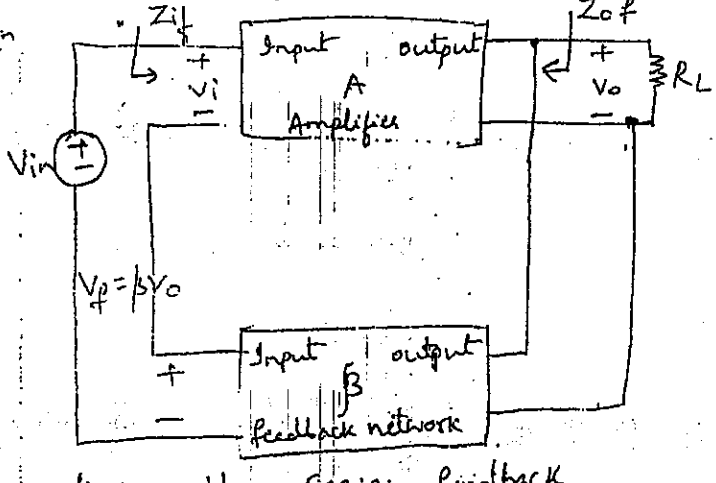


fig:- Voltage Series feedback

Explanation → 2M

from fig: $V_i = V_{in} - \beta V_o$

$V_o = AV_i = AV_{in} - A\beta V_o$

$V_o + A\beta V_o = AV_{in}$

$V_o(1 + A\beta) = AV_{in}$ → 3M

$\therefore$ $A_f = \frac{V_o}{V_{in}} = \frac{A}{1 + \beta A}$ → (1)

A : without f/b

A_f : with f/b → 1M

If $\beta A \gg 1$ eqn (1) reduces to

$A_f = \frac{1}{\beta}$ → (2)

Part D

7) Explain the construction and operation of N-channel JFET with their drain and transfer characteristics.

Soln:

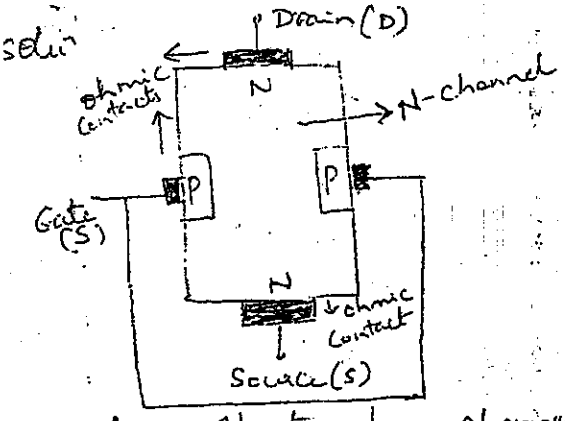


fig:- Structure of n-channel JFET

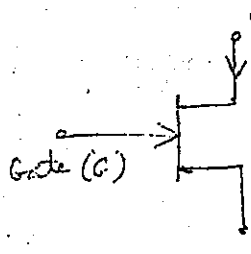
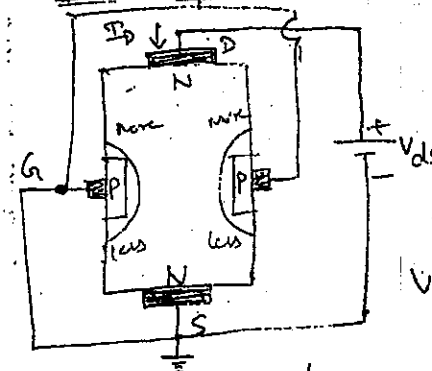
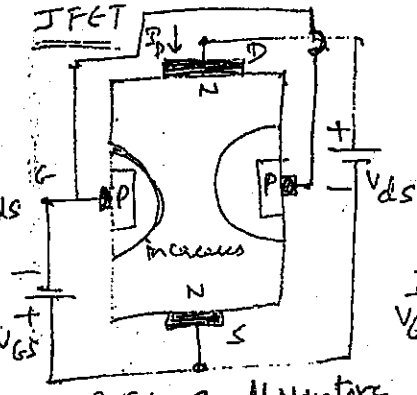


fig:- N-channel JFET Symbol

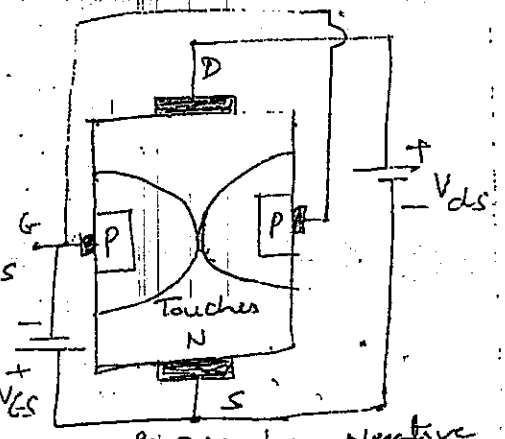
Working of n-Channel JFET



fig(a):- No bias v/g on gates, $V_{GS}=0$, $V_{ds}=+Ve$



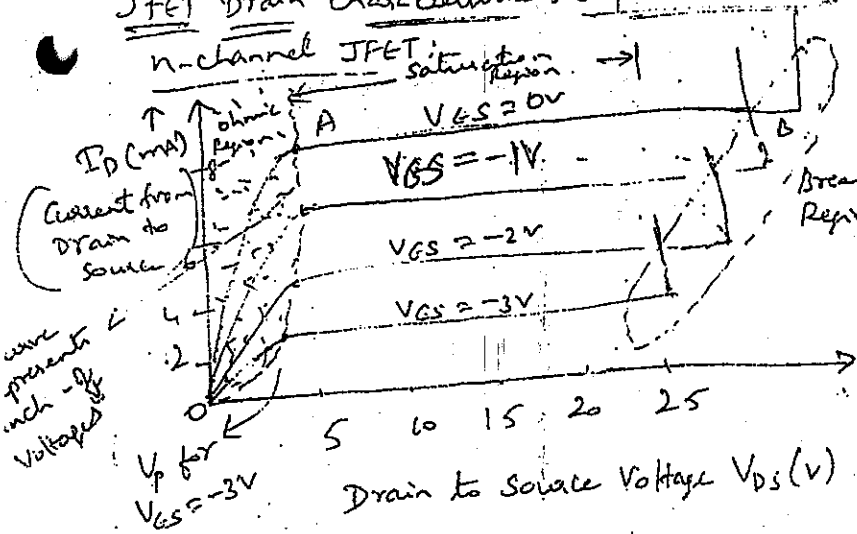
fig(b): Small Negative gate source bias
V_{GS} = -ve (low); V_{ds} = +ve



fig(c):- large Negative gate source bias
V_{GS} = -ve (high); V_{ds} = +ve

3M

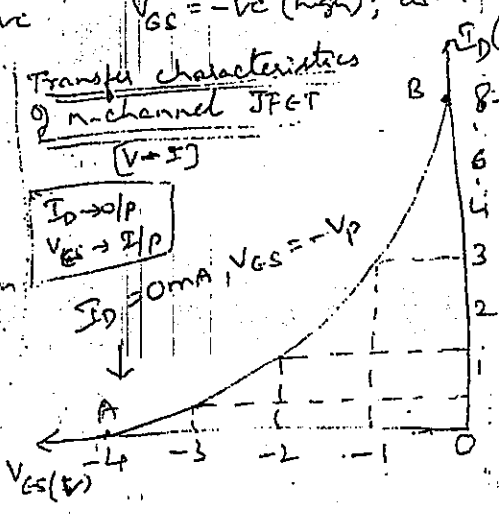
JFET Drain Characteristics: output characteristics



Transfer characteristics of n-channel JFET

[V→I]

I_D → o/p
V_{GS} → I/p



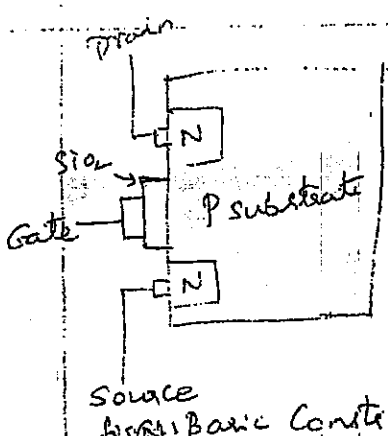
3M

Explanation → 2M

8) Explain the construction and operation of N-channel E-MOSFET with with their drain & transfer characteristics.

Soln:

Explanation →



fig(a): Basic Construction

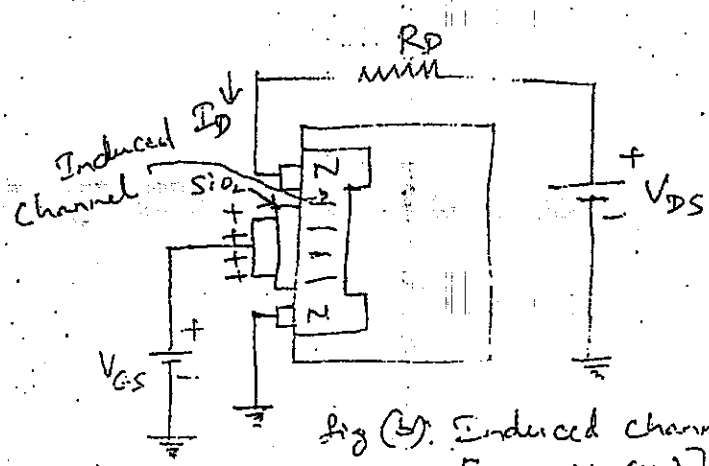
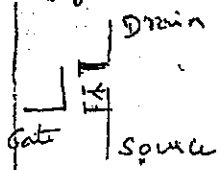


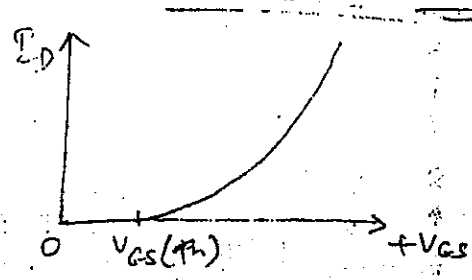
fig (b): Induced channel [$V_{GS} > V_{GS(Th)}$] N channel

3M



fig(c): Symbol of E-MOSFET (N channel)

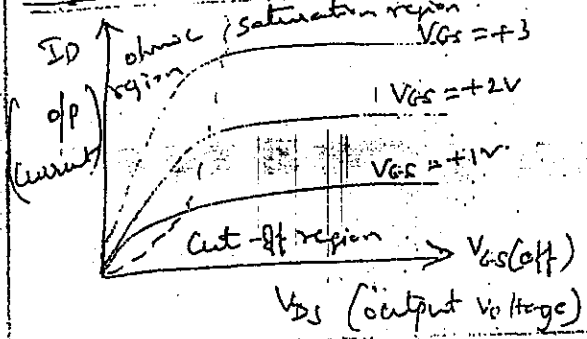
E-MOSFET: Transfer characteristics: N channel



$$I_D = K(V_{GS} - V_{GS(Th)})^2$$

3M

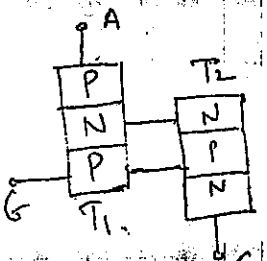
E-MOSFET: Drain characteristics: N channel



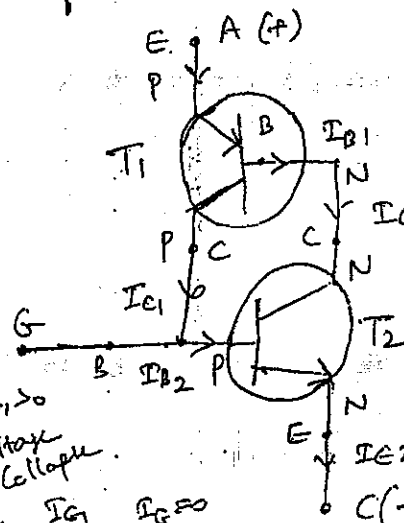
Part E

Q) Explain the two transistor model of SCR and also explain V-I Characteristics of SCR.

Soln



fig(a)



fig(b):

→ 3M

explanation → 3M

SCR Characteristics:

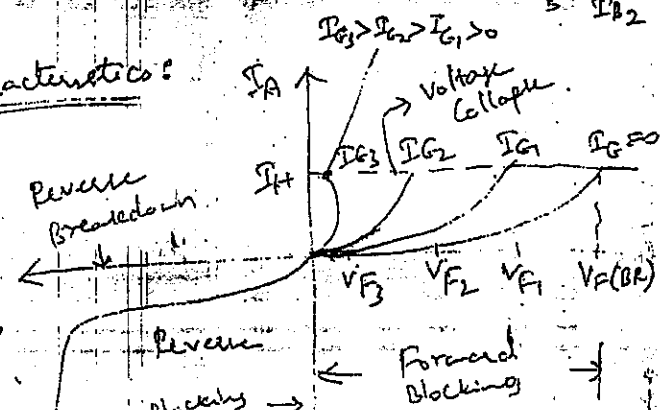
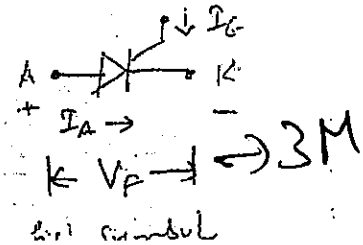


Fig:- V-I Characteristics



→ 3M

Fig: Symbol

10) a) $R = 10\,K\Omega$

$C = 1nF \qquad f_o = ?$

$R_o = 10\,K\Omega \qquad C = 1nF$

$$f_o = \frac{1}{2\pi R_C \sqrt{6}}$$

$$\frac{1}{2\pi (10\times 10^3)(1\times 10^{-19})\sqrt{6}}$$

$$f_o = 6.497\,kHz$$

b) $f = 300\,KHz \qquad R_1 = R_2 = 7.5\,K\Omega$

$$f = \frac{1.44}{(R_1 + 2R_2)C} = \frac{1.44}{(7.5R + 15k)C} = 300\times 10^3$$

$$C = \frac{1.44}{22.5\times 10^3 \times 300\times 10^3} \Longrightarrow \boxed{C = 0.213nF}$$

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IA-3 PERFORMANCE ANALYSIS

SUB: Basic Electronics — AY: 2020-21 (EVEN)

Course Code: 18ELN24 — Sem/Sec: 2B

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
Co Mapping	CO2	CO2	CO3	CO3	CO3	CO3	CO1	CO1	CO2	CO2
Max Marks for questions	6	6	6	6	6	6	6	6	6	6
Marks scored	114	185	30	268	276	22	154	150	174	123
no of students Attempted	19	31	5	45	46	4	26	25	29	21
60% of Max Marks for questions	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
no of students scored > 60% of marks/Question	19	31	5	45	46	4	26	25	29	21
Average no of students >60% of marks/Question	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Percentage	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00

Marks range	0-20	20 to 30
No. of Students	0	50

Staff Incharge
(Mrs. ASHWINI.K)

TUTORIAL ASSESSMENT REPORT 2020-21

Faculty: Mrs. Ashwini K **Subject** Basic Electronics

Code: 18ELN24 **SEM:** II **SEC:** B

Q1	Are you able to understand PN junction diodes and its applications?
Q2	Are you able to understand voltage regulators?
Q3	Are you able to describe the operation of JFET, MOSEFET?
Q4	Are you able to describe the characteristics of OP-amp and its applications?
Q5	Are you able to explain SCR and its applications?
Q6	Are you able to Explain Feedback amplifiers?
Q7	Are you able to Explain Oscillators and IC 555 timers?
Q8	Are you able to understand BJT as a switch and amplifier?
Q9	Are you able to solve fundamentals of Digital electronics, Combinational and sequential circuits?
Q10	Are you able to understand basic communication systems and operation of Mobile Phone?

CO	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
C128.1	Y	Y		Y			Y			
C128.2			Y	Y	Y			Y		
C128.3						Y	Y			
C128.4									Y	Y

R NO.	USN	Student name	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
B-01	3VC20CS107	Muskan	5	5	5	5	5	5	5	5	5	5
B-02	3VC20CS108	N R KARTHIKEYA	5	5	5	5	5	5	5	5	5	5
B-03	3VC20CS110	NADIRA ISURATH	5	5	5	5	5	5	5	5	5	5
B-04	3VC20CS111	NAGESH KUMAR B	5	5	5	5	5	5	5	5	5	5
B-05	3VC20CS112	NAVEED SUFIYAN P	5	5	5	5	5	5	5	5	5	5
B-07	3VC20CS114	NIDHI RAJSEKHAR MASGATTI MATH	5	5	5	5	5	5	5	5	5	5
B-08	3VC20CS115	NIKHIL JANEKUNTE	5	5	5	5	5	5	5	5	5	5
B-09	3VC20CS116	PARVATHI	5	5	5	5	5	5	5	5	5	5
B-10	3VC20CS011	PASUPULETI AISHWARYA	5	5	5	5	5	5	5	5	5	5
B-11	3VC20CS117	POOJARI PAVAN KUMAR	5	5	5	5	5	5	5	5	5	5
B-12	3VC20CS118	PRABHU M	5	5	5	5	5	5	5	5	5	5
B-13	3VC20CS119	PRADEEP KUMAR M	5	5	5	5	5	5	5	5	5	5
B-14	3VC20CS120	PRATHIK REDDY	5	5	5	5	5	5	5	5	5	5
B-15	3VC20CS121	PREETI LOKARE	5	5	5	5	5	5	5	5	5	5

B-16	3VC20CS122	PYATE SREE VENKATARAMANACHAR	5	5	5	5	5	5	5	5	5	5
B-17	3VC20CS123	R SANTOSH KUMAR	5	5	5	5	5	5	5	5	5	5
B-18	3VC20CS124	RAJASHEKAR B G	5	5	5	5	5	5	5	5	5	5
B-19	3VC20CS125	RAJASHEKAR D	5	5	5	5	5	5	5	5	5	5
B-20	3VC20CS127	RAVI KIRAN J	5	5	5	5	5	5	5	5	5	5
B-21	3VC20CS128	RAYANKULA CHANNAKESHAVA	5	5	5	5	5	5	5	5	5	5
B-22	3VC20CS129	REVATHI T	5	5	5	5	5	5	5	5	5	5
B-23	3VC20CS130	RITHIKA D	5	5	5	5	5	5	5	5	5	5
B-24	3VC20CS131	RITHVIK REDDY	5	5	5	5	5	5	5	5	5	5
B-25	3VC20CS132	S DEEPA	5	5	5	5	5	5	5	5	5	5
B-26	3VC20CS133	S KARTHIK	5	5	5	5	5	5	5	5	5	5
B-27	3VC20CS134	S NIZAM	5	5	5	5	5	5	5	5	5	5
B-28	3VC20CS135	S VIBHASHREE	5	5	5	5	5	5	5	5	5	5
B-29	3VC20CS136	SABA PARVEEN S	5	5	5	5	5	5	5	5	5	5
B-30	3VC20CS137	SADIQ MOHAMMED SIDDIQUI	5	5	5	5	5	5	5	5	5	5
B-31	3VC20CS138	SAHANA REDDY S	5	5	5	5	5	5	5	5	5	5
B-32	3VC20CS139	SAI NAYAN K	5	5	5	5	5	5	5	5	5	5
B-33	3VC20CS140	SAI TEJA T R	5	5	5	5	5	5	5	5	5	5
B-34	3VC20CS141	SAI THARUN G	5	5	5	5	5	5	5	5	5	5
B-35	3VC20CS142	SAINATH	5	5	5	5	5	5	5	5	5	5
B-36	3VC20CS143	SAKETH REDDY B	5	5	5	5	5	5	5	5	5	5
B-37	3VC20CS144	SANDHYA PATIL	5	5	5	5	5	5	5	5	5	5
B-38	3VC20CS145	SANGEETHA	5	5	5	5	5	5	5	5	5	5
B-39	3VC20CS146	SANGEETHA H	5	5	5	5	5	5	5	5	5	5
B-40	3VC20CS147	SANJANA A H M	5	5	5	5	5	5	5	5	5	5
B-41	3VC20CS148	SANTHOSH KUMAR C	5	5	5	5	5	5	5	5	5	5
B-42	3VC20CS149	SHAHID AFRIDI P	5	5	5	5	5	5	5	5	5	5
B-43	3VC20CS150	SHAIK MOHAMMED MUZAMMIL	5	5	5	5	5	5	5	5	5	5
B-44	3VC20CS151	SHASHANK D	5	5	5	5	5	5	5	5	5	5
B-45	3VC20CS152	SHASHANK T	5	5	5	5	5	5	5	5	5	5
B-46	3VC20CS153	SHEKSHAVALI P	5	5	5	5	5	5	5	5	5	5
B-47	3VC20CS154	SHIVARAMA REDDY K	5	5	5	5	5	5	5	5	5	5
B-48	3VC20CS155	SHWETHA K C	5	5	5	5	5	5	5	5	5	5
B-49	3VC20CS156	SIDDHARTH RUMALE	5	5	5	5	5	5	5	5	5	5
B-50	3VC20CS157	SINCHANA K	5	5	5	5	5	5	5	5	5	5
B-51	3VC20CS088	VINIT PRAKASH KHANDELWAL	5	5	5	5	5	5	5	5	5	5
0	0	0										
0	0	0										

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

2nd sem, B-Sec 2020-21 (Even)

FINAL INTERNAL, ASSINGMENT AND EXTERNAL MARKS

Sl No	USN	Name	Final IA Marks	Assignment Marks	External Exam Marks
1	3VC20CS107	MUSKAN	27	10	36
2	3VC20CS108	N R KARTHIKEYA	27	10	23
3	3VC20CS110	NADIRA ISURATH	28	10	32
4	3VC20CS111	NAGESH KUMAR B	29	10	33
5	3VC20CS112	NAVEED SUFIYAN P	27	10	29
6	3VC20CS114	NIDHI RAJSEKHAR MASGATTI MATH	28	10	29
7	3VC20CS115	NIKHIL JANEKUNTE	24	9	23
8	3VC20CS116	PARVATHI B	27	10	33
9	3VC20CS011	PASUPULETI AISHWARYA	29	10	23
10	3VC20CS117	POOJARI PAVAN KUMAR	27	10	28
11	3VC20CS118	PRABHU M	28	10	30
12	3VC20CS119	PRADEEP KUMAR M	28	10	31
13	3VC20CS120	PRATHIK REDDY	27	10	23
14	3VC20CS121	PREETI LOKARE	30	10	35
15	3VC20CS122	PYATE SREE VENKATARAMANACHAR	29	10	29
16	3VC20CS123	R SANTOSH KUMAR	27	10	27
17	3VC20CS124	RAJASHEKAR B G	29	10	39

18	3VC20CS125	RAJASHEKAR D	29	10	36
19	3VC20CS127	RAVI KIRAN J	29	10	33
20	3VC20CS128	RAYANKULA CHANNAKESHAVA	27	10	22
21	3VC20CS129	REVATHI T	27	10	28
22	3VC20CS130	RITHIKA D	27	10	31
23	3VC20CS131	RITHWIK REDDY	28	10	22
24	3VC20CS132	S DEEPA	29	10	36
25	3VC20CS133	S KARTHIK	29	10	40
26	3VC20CS134	S NIZAM	26	10	32
27	3VC20CS135	S VIBHASHREE	29	10	25
28	3VC20CS136	SABA PARVEEN S	27	10	37
29	3VC20CS137	SADIQ MOHAMMED SIDDIQUI	29	10	24
30	3VC20CS138	SAHANA REDDY S	29	10	37
31	3VC20CS139	SAI NAYAN K	29	10	38
32	3VC20CS140	SAI TEJA T R	28	10	20
33	3VC20CS141	SAI THARUN G	25	9	26
34	3VC20CS142	SAINATH	27	10	23
35	3VC20CS143	SAKETH REDDY B	29	10	38
36	3VC20CS144	SANDHYA PATIL	28	10	35
37	3VC20CS145	SANGEETHA	28	10	31
38	3VC20CS146	SANGEETHA H	28	10	29

39	3VC20CS147	SANJANA A H M	29	10	27
40	3VC20CS148	SANTHOSH KUMAR C	29	10	26
41	3VC20CS149	SHAHID AFRIDI P	22	8	6
42	3VC20CS150	SHAIK MOHAMMED MUZAMMIL	28	10	25
43	3VC20CS151	SHASHANK D	27	10	32
44	3VC20CS152	SHASHANK T	27	10	38
45	3VC20CS153	SHEKSHAVALI P	29	10	31
46	3VC20CS154	SHIVARAMA REDDY K	29	10	29
47	3VC20CS155	SHWETHA K C	27	10	26
48	3VC20CS156	SIDDHARTH RUMALE	29	10	34
49	3VC20CS157	SINCHANA K	30	10	26
50	3VC20CS088	VINIT PRAKASH KHANDELWAL	28	10	32

Head of the Department,
Electronics & Communication Engg.
R. Y. M. Engineering College
(Formerly ...)

Signature of faculty

Rao Bahadur Y Mahabaleswarappa Engineering College

Department of Electronics & Communication Engineering

Semester : 2 / B **Course Exit Survey 2020-21**

Course Name: BASIC ELECTRONICS **Cours code:18ELN24**

Course Outcomes: After studying this course, the students will be

C128.1	Describe the operation, characteristics of diodes, FETs, SCR, Operational amplifiers, IC regulators, astable oscillator using 555 timers and Communication Systems.
C128.2	Explain the applications of diodes, BJT, SCR, and Operational amplifiers.
C128.3	Describe Oscillators and feedback amplifiers.
C128.4	Explain the different types of number systems; construct the combinational and sequential circuits using flip flops.

Please grade the course Outcomes with appropriate one :

Excellent – 5, Very Good – 4, Good – 3,Average – 2, Below Average - 1

Sl. No	USN	Name of the Student	C128.1	C128.2	C128.3	C128.4	Sign
B-01	3VC20CS107	MUSKAN	5	4	4	5	
B-02	3VC20CS108	N R KARTHIKEYA	5	4	5	5	
B-03	3VC20CS110	NADIRA ISURATH	4	5	5	4	
B-04	3VC20CS111	NAGESH KUMAR B	5	5	4	5	
B-05	3VC20CS112	NAVEED SUFIYAN P	5	4	5	4	
B-06	3VC20CS113	NAZNEEN					
B-07	3VC20CS114	MATH	5	5	4	5	
B-08	3VC20CS115	NIKHIL JANEKUNTE	4	5	5	5	
B-09	3VC20CS116	PARVATHI B	5	5	5	5	
B-10	3VC20CS011	PASUPULETI AISHWARYA	5	5	4	5	
B-11	3VC20CS117	POOJARI PAVAN KUMAR	5	5	5	5	
B-12	3VC20CS118	PRABHU M	5	5	5	5	
B-13	3VC20CS119	PRADEEP KUMAR M	5	5	5	5	
B-14	3VC20CS120	PRATHIK REDDY	5	4	5	5	
B-15	3VC20CS121	PREETI LOKARE	5	5	5	5	
B-16	3VC20CS122	VENKATARAMANACHAR	5	4	4	5	
B-17	3VC20CS123	R SANTOSH KUMAR	5	5	5	5	
B-18	3VC20CS124	RAJASHEKAR B G	5	5	5	5	
B-19	3VC20CS125	RAJASHEKAR D	5	5	5	5	
B-20	3VC20CS127	RAVI KIRAN J	5	5	5	5	
B-21	3VC20CS128	RAYANKULA CHANNAKESHAVA	4	5	5	5	
B-22	3VC20CS129	REVATHI T	5	4	5	4	
B-23	3VC20CS130	RITHIKA D	5	4	5	4	
B-24	3VC20CS131	RITHVIK REDDY	5	5	5	4	
B-25	3VC20CS132	S DEEPA	5	4	5	4	
B-26	3VC20CS133	S KARTHIK	5	4	5	4	
B-27	3VC20CS134	S NIZAM	5	4	5	4	
B-28	3VC20CS135	S VIBHASHREE	4	5	5	4	
B-29	3VC20CS136	SABA PARVEEN S	5	4	5	5	

Sl. No.	USN	Name of the Student	C128.1	C128.2	C128.3	C128.4	Sign
B-30	3VC20CS137	SIDDIQUI	5	5	5	5	
B-31	3VC20CS138	SAHANA REDDY S	5	5	5	5	
B-32	3VC20CS139	SAI NAYAN K	5	4	5	4	
B-33	3VC20CS140	SAI TEJA T R	5	5	5	5	
B-34	3VC20CS141	SAI THARUN G	4	5	5	5	
B-35	3VC20CS142	SAINATH	5	4	5	4	
B-36	3VC20CS143	SAKETH REDDY B	5	4	5	4	
B-37	3VC20CS144	SANDHYA PATIL	5	5	5	4	
B-38	3VC20CS145	SANGEETHA	5	5	5	5	
B-39	3VC20CS146	SANGEETHA H	5	5	5	5	
B-40	3VC20CS147	SANJANA A H M	5	5	5	5	
B-41	3VC20CS148	SANTHOSH KUMAR C	5	5	4	5	
B-42	3VC20CS149	SHAHID AFRIDI P	5	5	5	5	
B-43	3VC20CS150	MUZAMMIL	5	4	5	5	
B-44	3VC20CS151	SHASHANK D	5	5	5	5	
B-45	3VC20CS152	SHASHANK T	5	4	5	5	
B-46	3VC20CS153	SHEKSHAVALI P	5	5	4	5	
B-47	3VC20CS154	SHIVARAMA REDDY K	5	4	5	4	
B-48	3VC20CS155	SHWETHA K C	5	5	5	5	
B-49	3VC20CS156	SIDDHARTH RUMALE	5	5	4	5	
B-50	3VC20CS157	SINCHANA K	5	5	4	5	
B-51	3VC20CS088	KHANDELWAL	5	5	5	5	

Staff Incharge

Mrs. ASHWINI.K

Rao Bahadur Y Mahabaleswarappa Engineering College

Department of Electronics & Communication Engineering

Semester : 2 / B COURSE SELF ASSESSMENT REPORT 2020-21

Course Name: BASIC ELECTRONICS **Cours code:18ELN24**

Questionnaires for BASIC ELECTRONICS 18ELN24

1	Are you able to understand PN junction diodes and its applications?
2	Are you able to understand voltage regulators?
3	Are you able to describe the operation of JFET, MOSEFET?
4	Are you able to describe the characteristics of OP-amp and its applications?
5	Are you able to explain SCR and its applications?
6	Are you able to Explain Feedback amplifiers?
7	Are you able to Explain Oscillators and IC 555 timers?
8	Are you able to understand BJT as a switch and amplifier?
9	Are you able to solve fundamentals of Digital electronics, Combinational and sequential circuits?
10	Are you able to understand basic communication systems and operation of Mobile Phone?
Guidelines: Excellent – 5, Very Good – 4, Good – 3,Average – 2, Below Average - 1	

Sl. No	USN NO	Name of the Student	ELN-18ELN24- Questionaire No										Signature
			1	2	3	4	5	6	7	8	9	10	
B-01	3VC20CS107	MUSKAN	4	5	5	4	4	5	4	5	5	4	
B-02	3VC20CS108	N R KARTHIKEYA	5	5	5	4	5	5	4	4	4	5	
B-03	3VC20CS110	NADIRA ISURATH	5	5	4	4	5	5	4	5	4	5	
B-04	3VC20CS111	NAGESH KUMAR B	5	5	5	5	5	4	0	4	5	5	
B-05	3VC20CS112	NAVEED SUFIYAN P	5	5	5	5	5	5	5	5	5	5	
B-06	3VC20CS113	NAZNEEN											
B-07	3VC20CS114	MASGATTI MATH	5	5	5	5	5	5	5	5	5	5	
B-08	3VC20CS115	NIKHIL JANEKUNTE	4	5	5	5	5	5	5	5	5	4	
B-09	3VC20CS116	PARVATHI B	5	5	5	5	5	5	5	5	5	5	
B-10	3VC20CS011	AISHWARYA	5	5	4	5	5	4	5	5	5	4	
B-11	3VC20CS117	KUMAR	5	5	5	5	5	5	5	5	5	5	
B-12	3VC20CS118	PRABHU M	5	5	5	5	5	5	5	5	5	5	
B-13	3VC20CS119	PRADEEP KUMAR M	5	5	5	5	5	5	5	5	5	5	
B-14	3VC20CS120	PRATHIK REDDY	5	5	5	4	5	5	4	5	5	5	
B-15	3VC20CS121	PREETI LOKARE	5	5	5	5	5	5	5	5	5	5	
B-16	3VC20CS122	VENKATARAMANACHA	5	4	5	4	5	5		4	5	4	

B-17	3VC20CS123	R SANTOSH KUMAR	5	5	5	5	5	5	5	5	5	5	
B-18	3VC20CS124	RAJASHEKAR B G	5	5	5	5	5	5	5	5	5	5	
B-19	3VC20CS125	RAJASHEKAR D	5	5	5	5	5	5	5	5	5	5	
B-20	3VC20CS127	RAVI KIRAN J	5	5	5	5	5	5	5	5	5	5	
B-21	3VC20CS128	CHANNAKESHAVA	5	5	5	5	4	5	5	4	5	5	
B-22	3VC20CS129	REVATHI T	5	4	5	4	5	4	5	5	5	5	
B-23	3VC20CS130	RITHIKA D	5	4	5	5	5	5	5	5	5	5	
B-24	3VC20CS131	RITHVIK REDDY	5	5	4	5	5	4	5	5	5	5	
B-25	3VC20CS132	S DEEPA	5	5	5	5	5	5	5	4	4	5	
B-26	3VC20CS133	S KARTHIK	5	4	5	4	5	4	5	4	5	4	
B-27	3VC20CS134	S NIZAM	5	4	5	4	5	4	5	4	5	4	
B-28	3VC20CS135	S VIBHASHREE	5	4	5	4	5	4	5	4	5	4	
B-29	3VC20CS136	SABA PARVEEN S	5	4	5	4	5	4	5	5	4	4	
B-30	3VC20CS137	SIDDIQUI	5	5	5	5	5	5	5	5	5	5	
B-31	3VC20CS138	SAHANA REDDY S	5	5	5	5	4	4	4	5	5	5	
B-32	3VC20CS139	SAI NAYAN K	5	4	4	5	5	4	5	5	4	5	
B-33	3VC20CS140	SAI TEJA T R	5	4	5	5	5	4	5	5	5	5	
B-34	3VC20CS141	SAI THARUN G	4	5	5	5	5	4	5	5	5	5	
B-35	3VC20CS142	SAINATH	5	4	5	4	5	4	5	4	5	4	
B-36	3VC20CS143	SAKETH REDDY B	5	5	5	5	5	5	5	5	5	5	
B-37	3VC20CS144	SANDHYA PATIL	5	5	5	5	5	5	5	5	5	5	
B-38	3VC20CS145	SANGEETHA	5	5	5	5	5	5	5	5	5	5	
B-39	3VC20CS146	SANGEETHA H	5	5	5	5	5	4	4	4	4	4	
B-40	3VC20CS147	SANJANA A H M	5	5	5	5	5	5	5	5	5	5	
B-41	3VC20CS148	SANTHOSH KUMAR C	5	5	5	5	4	5	4	5	5	5	
B-42	3VC20CS149	SHAHID AFRIDI P	5	5	5	5	5	5	5	5	5	5	
B-43	3VC20CS150	MUZAMMIL	5	5	5	5	5	4	5	4	5	5	
B-44	3VC20CS151	SHASHANK D	5	5	5	5	5	5	4	5	5	5	
B-45	3VC20CS152	SHASHANK T	5	5	5	4	4	6	5	5	5	5	
B-46	3VC20CS153	SHEKSHAVALI P	5	5	5	5	5	5	4	4	5	5	
B-47	3VC20CS154	SHIVARAMA REDDY K	5	5	5	5	5	5	5	5	5	5	
B-48	3VC20CS155	SHWETHA K C	5	5	5	5	5	5	5	5	5	5	
B-49	3VC20CS156	SIDDHARTH RUMALE	5	4	5	4	5	4	5	4	5	4	
B-50	3VC20CS157	SINCHANA K	5	4	5	4	5	4	5	4	5	4	
B-51	3VC20CS088	KHANDELWAL	5	5	5	5	4	5	5	4	5	5	

Staff Incharge
MRS. ASHWINI K

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGNEERING

DIRECT ATTAINMENT 2020-21

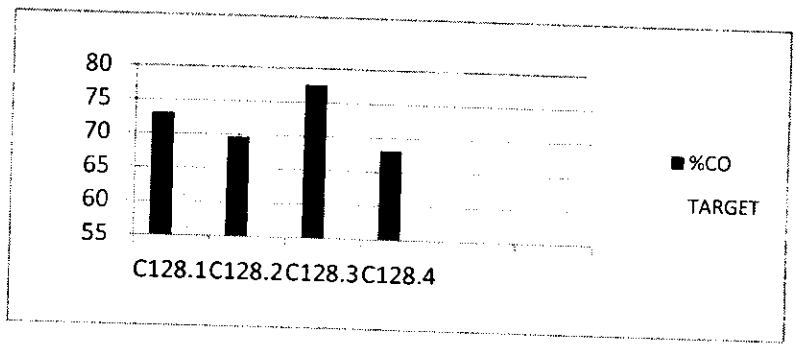
Faculty: Mrs. Ashwini K **Code:** 18ELN24
Subject: Basic Electronics
SEM: II **SEC:** B

COURSE OUTCOME STATEMENT	
C128.1	Describe the operation, characteristics of diodes, FETs, SCR, Operational amplifiers, IC regulators, astable oscillator using 555 timers and Communication Systems.
C128.2	Explain the applications of diodes, BJT, SCR, and Operational amplifiers.
C128.3	Describe Oscillators and feedback amplifiers.
C128.4	Explain the different types of number systems; construct the combinational and sequential circuits using flip flops.

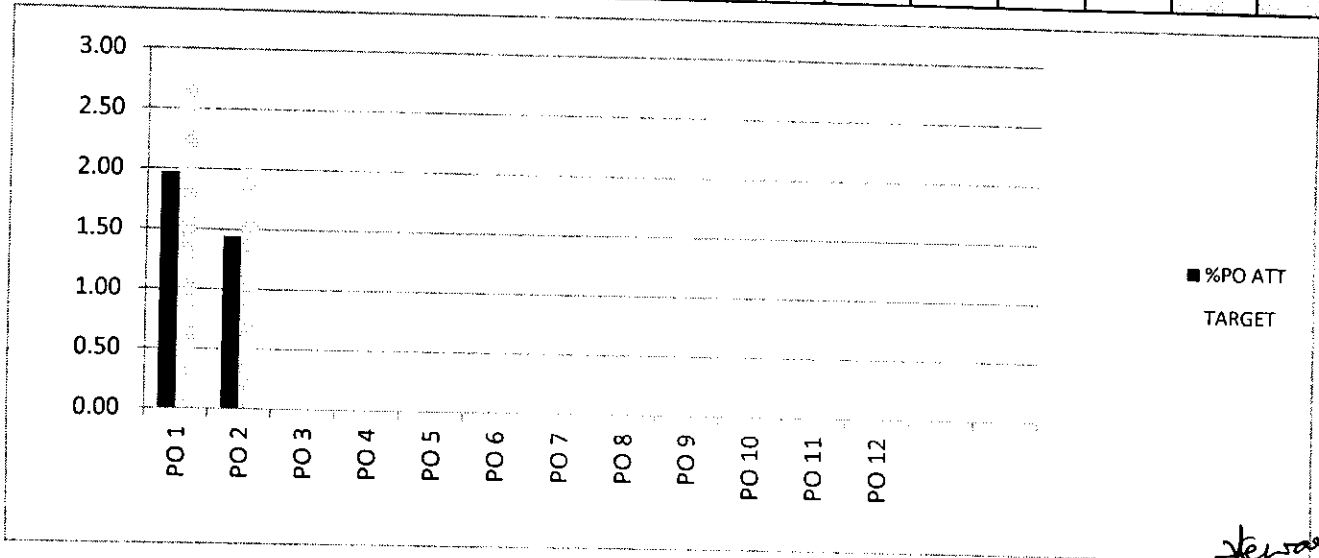
CO-PO Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12		
C128.1	3	2	0	0	0	0	0	0	0	0	0	0		
C128.2	3	2	0	0	0	0	0	0	0	0	0	0		
C128.3	2	2	0	0	0	0	0	0	0	0	0	0		
C128.4	3	2	0	0	0	0	0	0	0	0	0	0		

	%CO	TARGET
C128.1	73.09	65
C128.2	69.73	65
C128.3	77.6	65
C128.4	68.17	65



	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12		
%PO ATT	1.97	1.44												
TARGET	2.75	2												



Staff Incharge
MRS. ASHWINI.K

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGNEERING

INDIRECT ATTAINMENT 2020-21

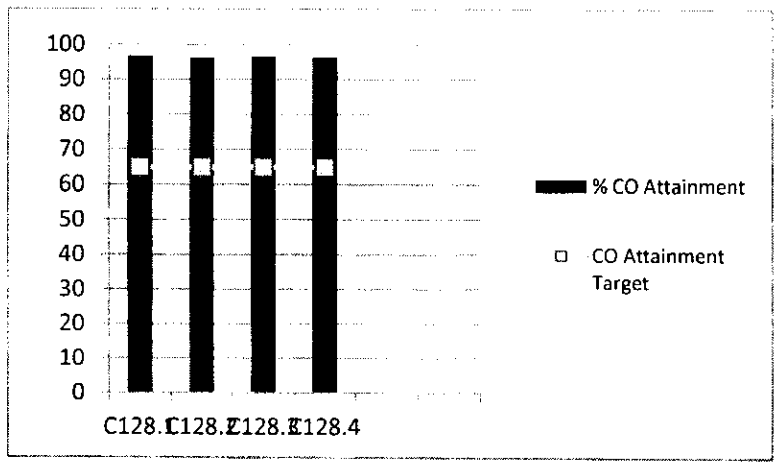
Faculty: Mrs. Ashwini K **Code:** 18ELN24
Subject: Basic Electronics
SEM: II **SEC:** B

COURSE OUTCOME STATEMENT	
C128.1	Describe the operation, characteristics of diodes, FETs, SCR, Operational amplifiers, IC regulators, astable oscillator using 555 timers and Communication Systems.
C128.2	Explain the applications of diodes, BJT, SCR, and Operational amplifiers.
C128.3	Describe Oscillators and feedback amplifiers.
C128.4	Explain the different types of number systems; construct the combinational and sequential

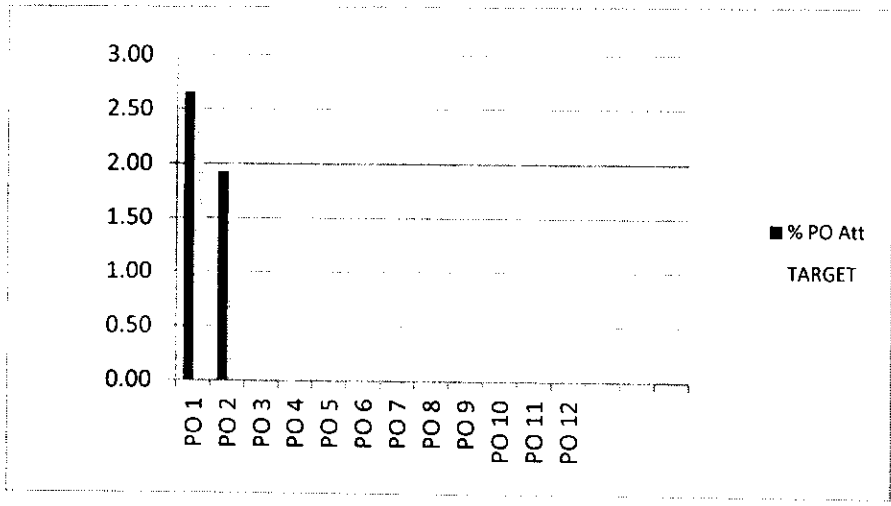
CO-PO Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12		
C128.1	3	2	0	0	0	0	0	0	0	0	0	0		
C128.2	3	2	0	0	0	0	0	0	0	0	0	0		
C128.3	2	2	0	0	0	0	0	0	0	0	0	0		
C128.4	3	2	0	0	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0	0	0	0	0		

	% CO Attainment	CO Attainment Target
C128.1	96.8	65
C128.2	96.27	65
C128.3	96.67	65
C128.4	96.4	65



PO's	% PO Att	TARGET
PO 1	2.65	2.75
PO 2	1.93	2
PO 3		
PO 4		
PO 5		
PO 6		
PO 7		
PO 8		
PO 9		
PO 10		
PO 11		
PO 12		



Staff Incharge
(MRS. ASHWINI.K)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SUB: Basic Electronics

AY: 2020-21 (EVEN)

Course Code: 18ELN24

Sem/Sec: 2B

CO ATTAINMENT GAP ANALYSIS 2020-21

Course Outcomes	CO Attainment	CO Target	CO Attainment gap
C114.1	73.09	65	Attained (No Gap)
C114.2	69.73	65	Attained (No Gap)
C114.3	77.6	65	Attained (No Gap)
C114.4	68.17	65	Attained (No Gap)

ACTION REPORT ON GAP ANALYSIS

Course Outcomes	Action Proposed to bridge the gap	Modification of Target if achieved
C114.1	–	67
C114.2	–	67
C114.3	–	67
C114.4	–	67

Staff Incharge
(MRS. ASHWINI.K)

INSTRUCTOR REPORT: 2020-21 (EVEN SEM)

Impact of Delivery Methods (State the delivery methods used and its effectiveness):

- **Blended method**: This subject was taught in blended mode both in offline and online mode due to pandemic again for the second time; offline teaching method was effective compared to online teaching. In online teaching shared presentations, done live classes using white board (Jamboard App.), sent digital notes on high priority in Google classrooms and Google meet platforms.

- **Teaching-Learning**: After teaching each module students are assigned with assignments. After completion of all modules, conducted quiz through Google form and issued certificates to students who scored more than 60% to motivate students and for better understanding of the topic which is outcome based knowledge i.e student rather than just remembering the concepts and reproducing in exams, now students were started thinking and applying the knowledge and analyzing, presenting skills were improved.

Course Outcome Attainment Remarks: All Course outcomes are attained.

Instructor Feedback: Overall the Basic Electronics is the fundamental course which enhances the student's ability to learn, understand and applying the concepts. Hence student's centric approach is adapted to exhibit teaching methodologies.

Scope for **improvement:** Overall this subject attainment increases if we use outcome based student centric approach which reflects in securing good score as well gaining knowledge which is directly proportional to improvements in attainment levels.

Staff Incharge
(Mrs. ASHWINI.K)

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics & Communication Engineering

Innovative Practice / Best Practice

Title of the Practice:

"Quiz through Google Form" Certificates will be issued to students who scored more than 60%

1. **Goal:**
   - Students will gain the knowledge on Semiconductors, Diodes, Zener Diodes, Operational Amplifiers, FET, Oscillators & Rectifiers, Digital Electronics, Feedback Amplifiers etc.
   - We can gauge the students engagement in learning process
   - To reach every students
   - Issuing Certificates to Motivate Students.
2. **The context :**

   Students are learning **Basic Electronics Course** 2nd semester course in the VTU curriculum. Video & Live lecture of "Semiconductors, Diodes, Zener Diodes, Operational Amplifiers, FET, Oscillators & Rectifiers, Digital Electronics, Feedback Amplifiers etc." topics were taught and conducted **"Quiz through Google Form"** and **Issued Certificates** to students who scored more than **60%** to motivate students and for the better understanding of the topic.

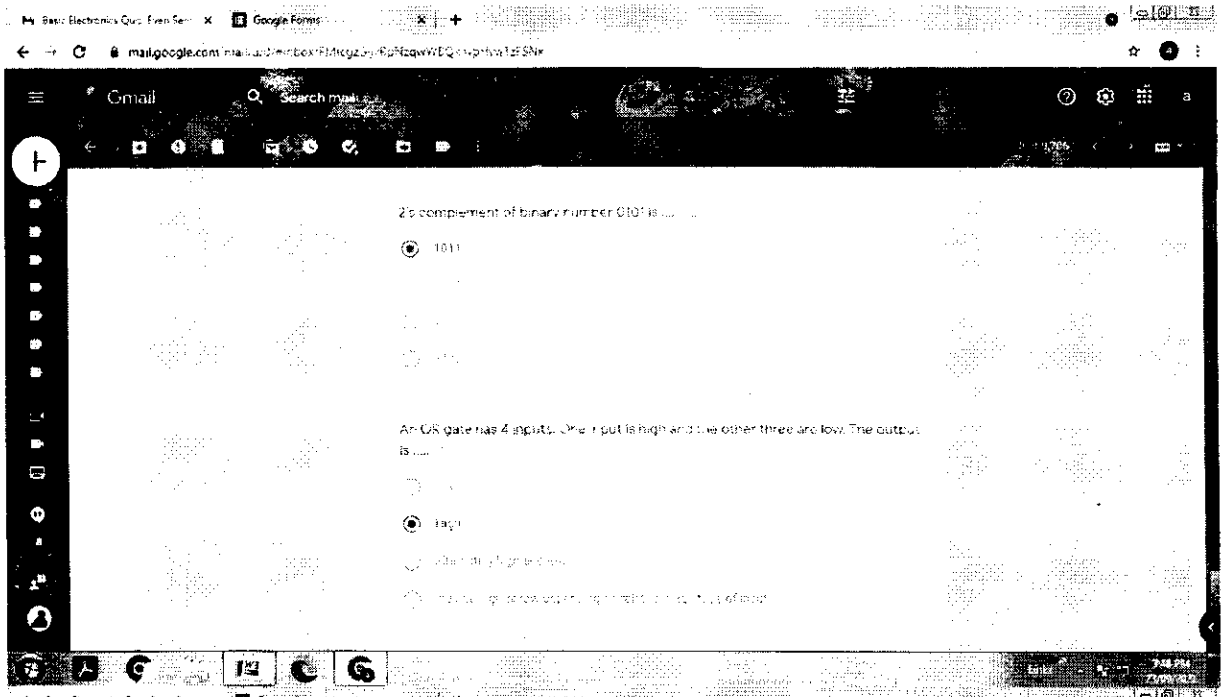
The Practice:

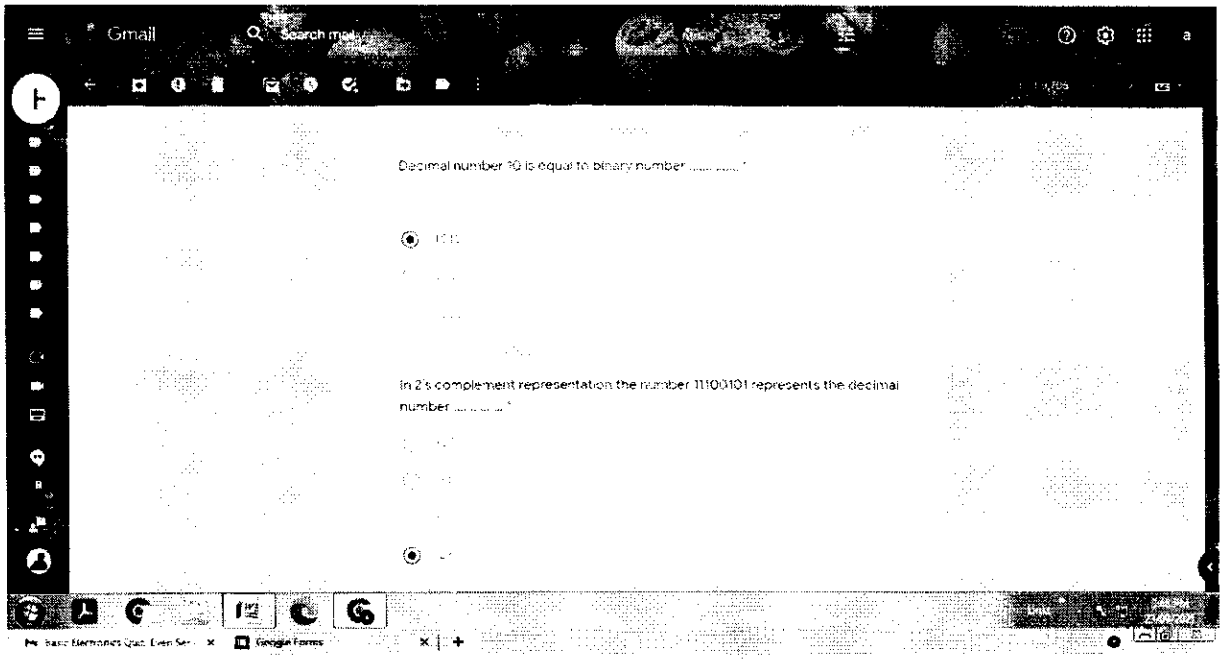
- Students need to prepare the basic electronics course by study material provided, they should come live to E-class through Google meet app and they can clarify their doubts in Google Classes/Google meet, Whatsapp or any other e-learning mode platforms. Conducted Quiz for Self Assessment and to motivate students issued certificates. GMeet app practice will provide interactive sessions.

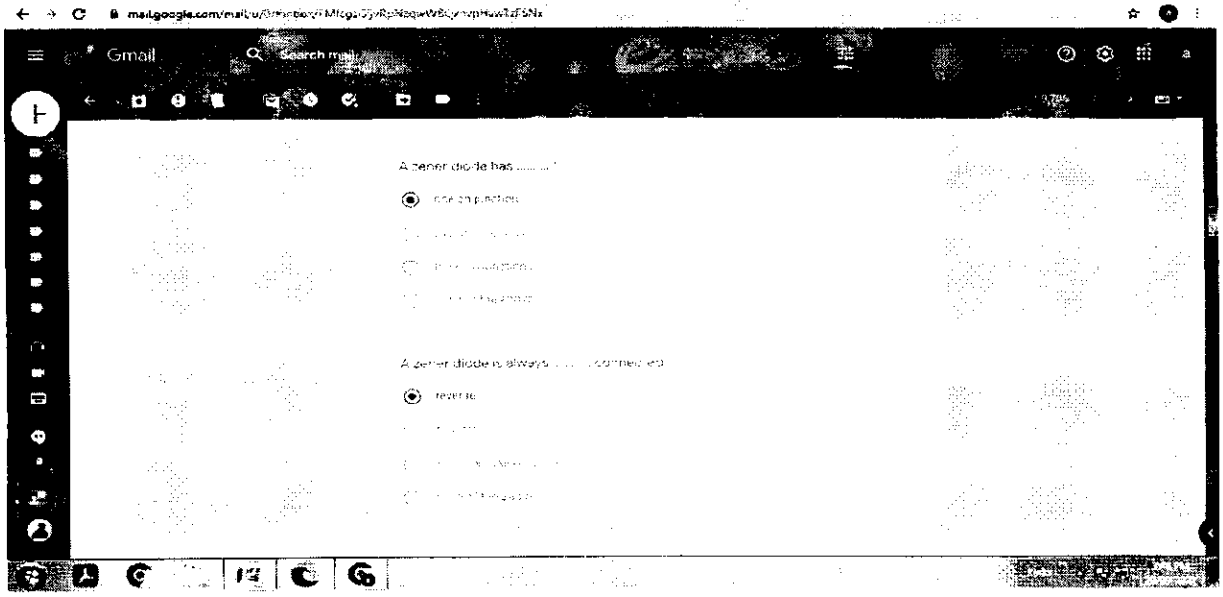
Mrs. Ashwini K

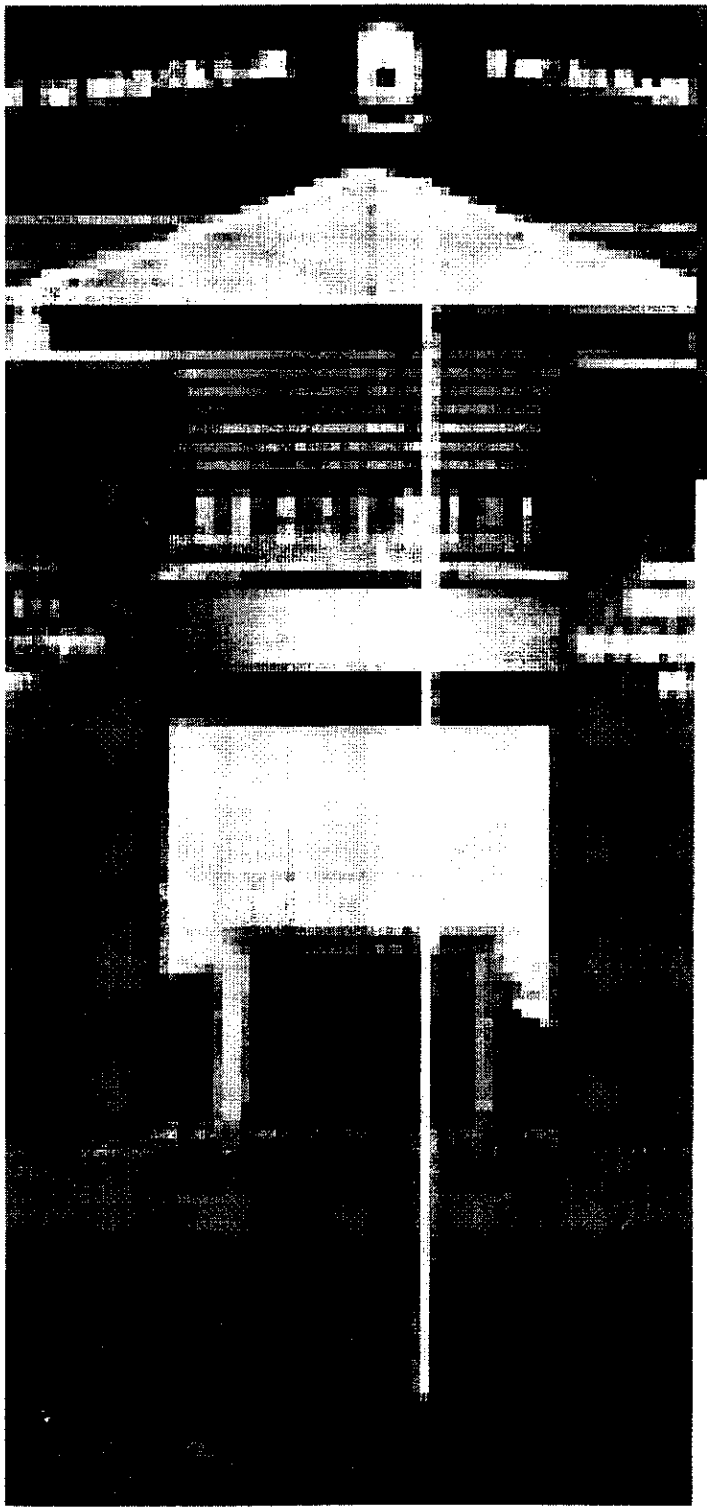
Staff Incharge

HOD


Gmail
2's complement of binary number 0101 is .....
1011
An OR gate has 4 inputs. One input is high and the other three are low. The output is .....
high


Gmail
Decimal number 10 is equal to binary number .....
1010
In 2's complement representation the number 11100101 represents the decimal number .....
-27


Gmail
A zener diode has .....
A zener diode is always .....
reverse



V.V.Sangha's

Rao Bahadur Y. Mahabaleswarappa Engineering College, Ballari.

Department of Electronics & Communication Engineering

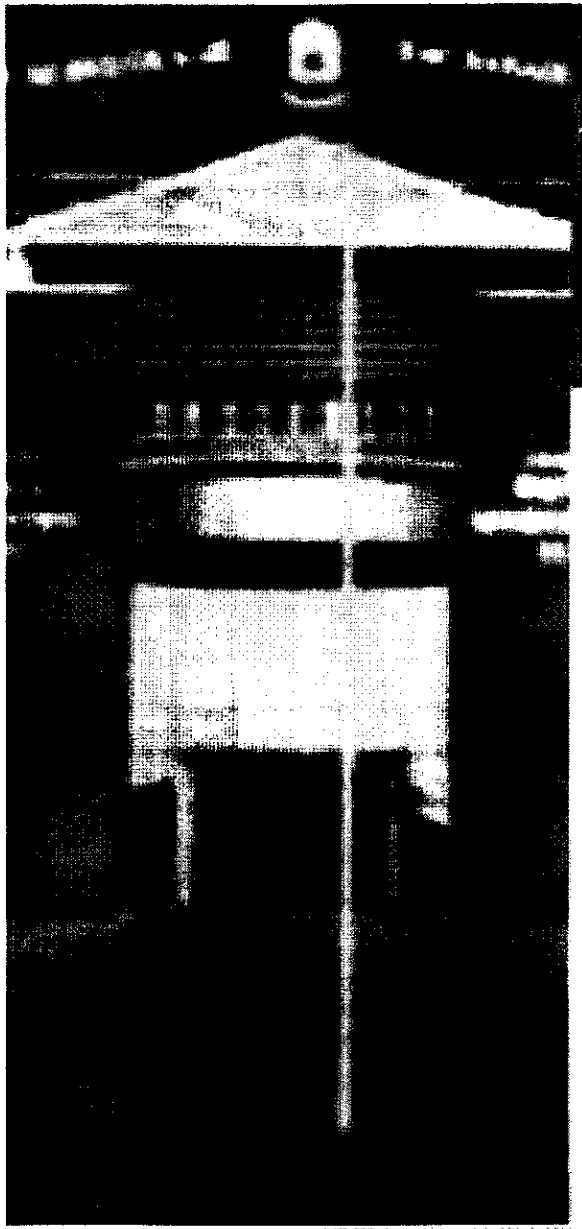
CERTIFICATE OF PARTICIPATION

This is to Certify that Saketh Reddy B Bearing USN 3VC20CS143 From Rao Bahadur Y.Mahabaleswarappa Engineering College Has Participated in "BASIC ELECTRONICS QUIZ 2021" Organised by Department of Electronics & Communication Engineering, RYMEC, Ballari on September 2021.

DR. T. HANUMANTHA REDDY
Principal

DR. SAVITA SONOLI
Vice Principal & HOD-ECE

Co-ordinator: Mrs. Ashwini K
Asst. Professor
Dept. of E&CE



V.V.Sangha's
Rao Bahadur Y. Mahabaleswarappa
Engineering College, Ballari.

Department of Electronics & Communication Engineering

CERTIFICATE OF PARTICIPATION

This is to Certify that** Parvathi.B **Bearing USN** 3VC20CS116 **From** RAO BAHADUR Y MAHABALESHWARAPPA ENGINEERING COLLEGE **Has Participated in** "BASIC ELECTRONICS QUIZ 2021" **Organised by Department of Electronics & Communication Engineering, RYMEC, Ballari on September 2021.

DR. T HANUMANTHA REDDY
Principal

DR. SAVITA SONOLI
Vice Principal & HOD-ECE

ECE

Co-ordinator: Mrs. Ashwini K
Asst. Professor
Dept. of E&CE

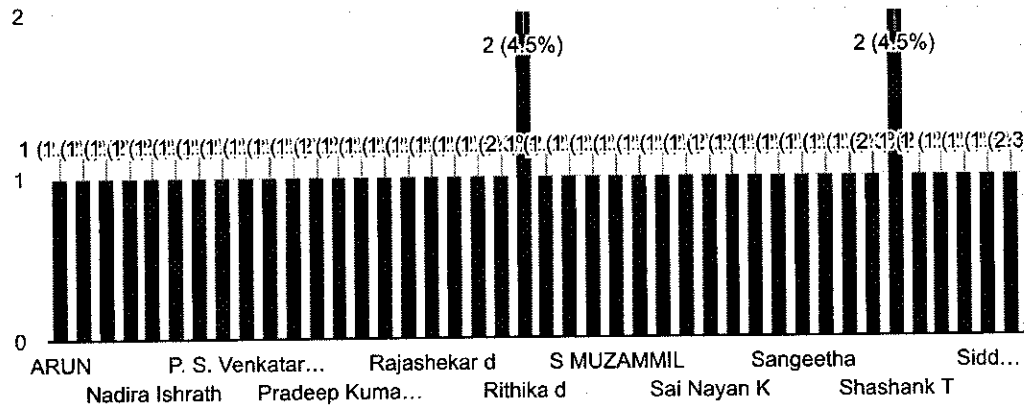
Basic Electronics Quiz, Even Sem, 2020-21

44 responses

Publish analytics

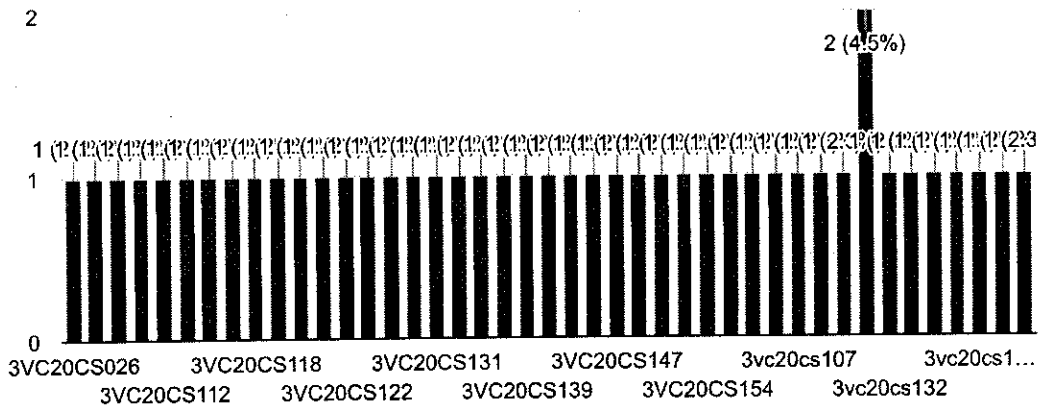
Name of the Student

44 responses



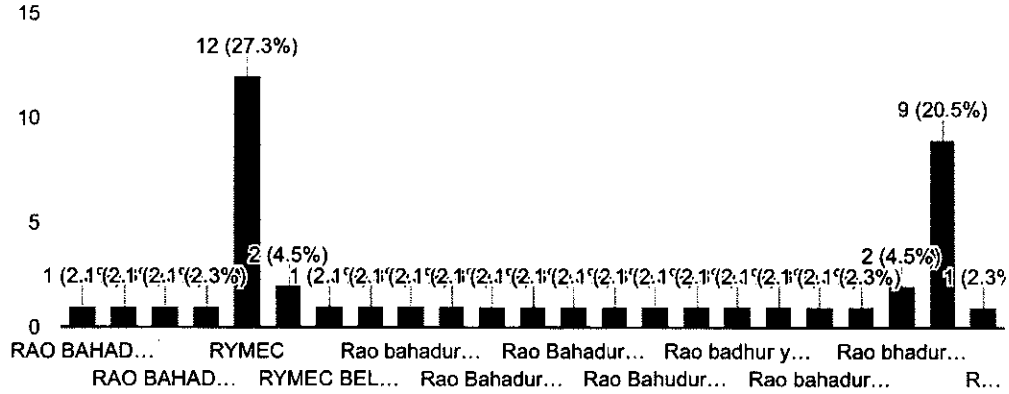
USN

44 responses



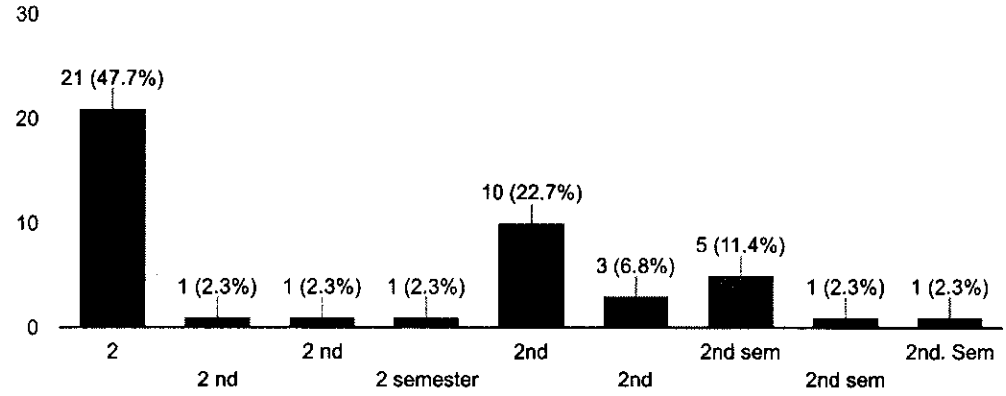
Institution Name

44 responses



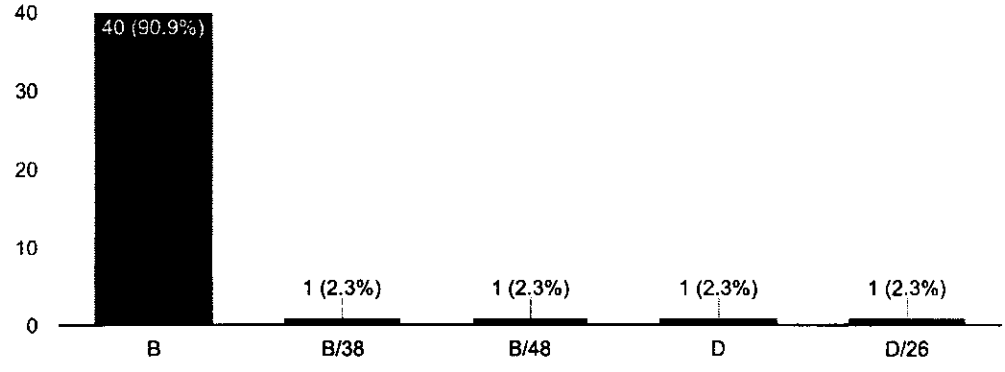
Semester

44 responses



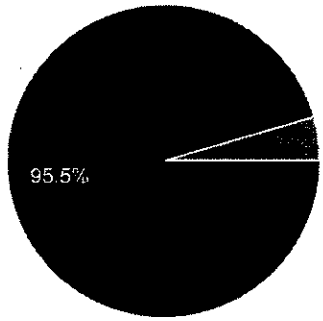
Section

44 responses



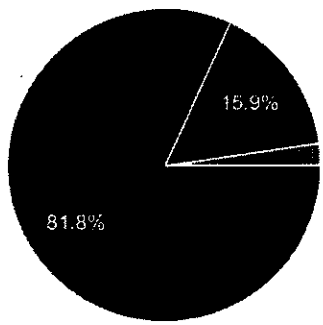
A zener diode is used as .....

44 responses



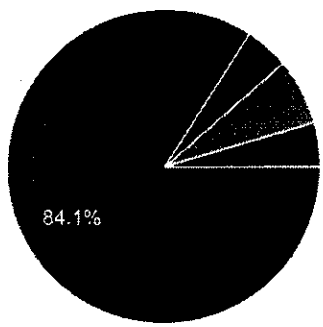
A zener diode has .....

44 responses



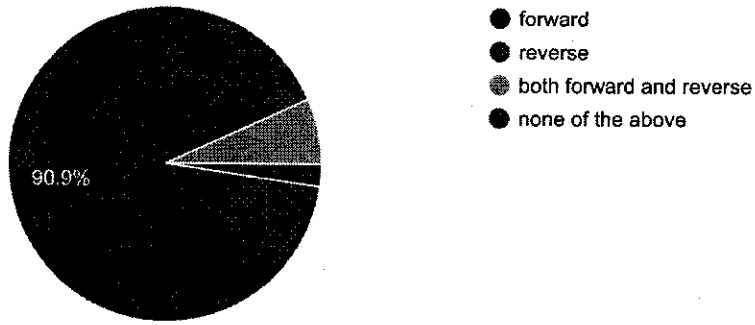
A zener diode is always ..... connected.

44 responses



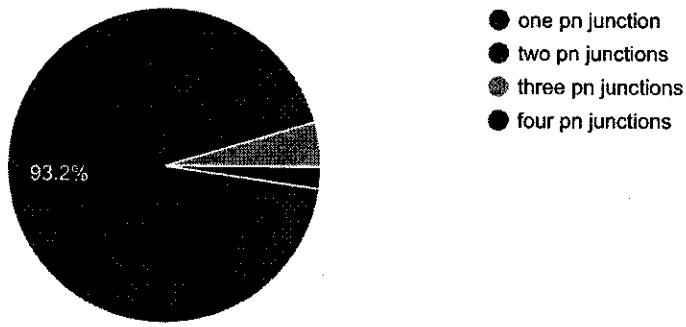
A zener diode utilizes ..... characteristics for its operation.

44 responses



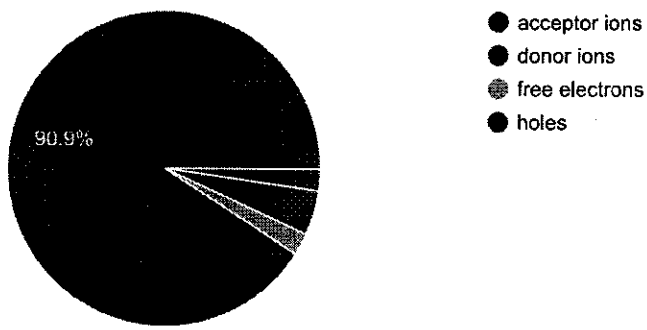
A transistor has .....

44 responses



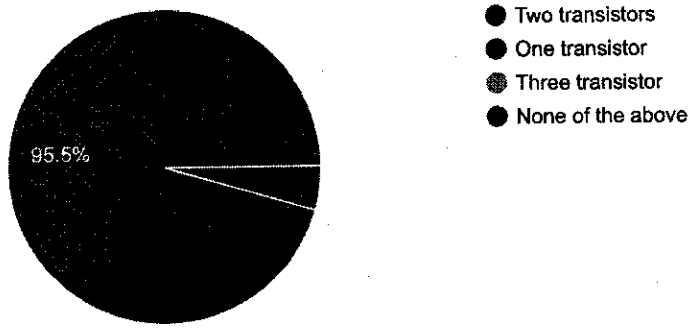
In a pnp transistor, the current carriers are .....

44 responses



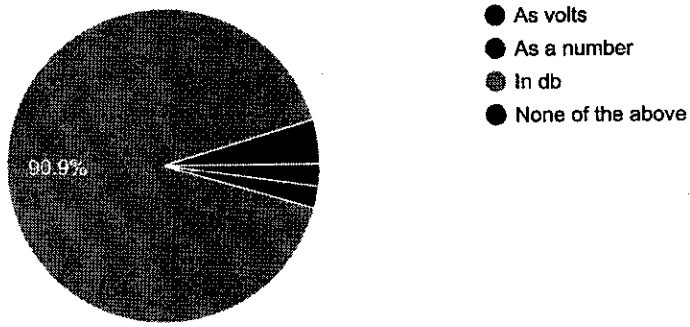
A single stage transistor amplifier contains ..... and associated circuitry

44 responses



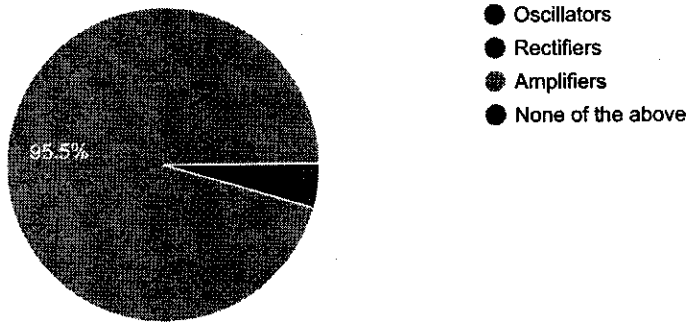
In practice, the voltage gain of an amplifier is expressed .....

44 responses



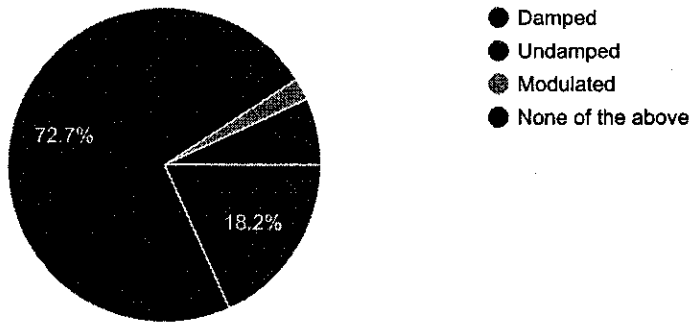
Negative feedback is employed in .....

44 responses



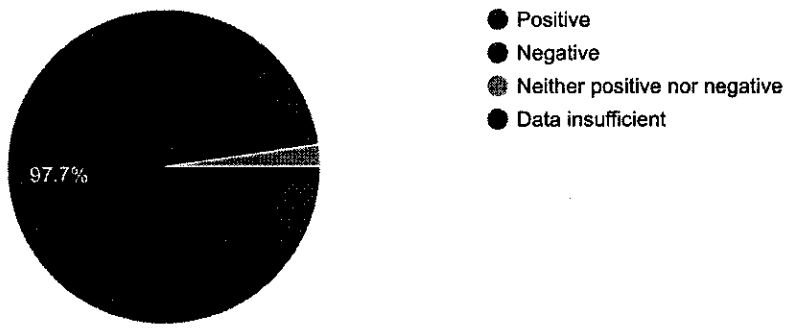
An oscillator produces..... oscillations

44 responses



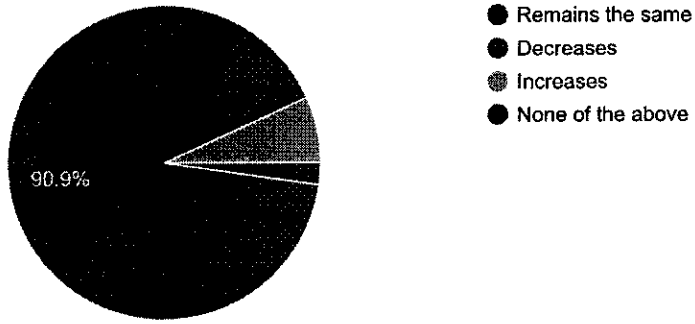
An oscillator employs ..... feedback

44 responses



In an unregulated power supply, if load current increases, the output voltage .....

44 responses



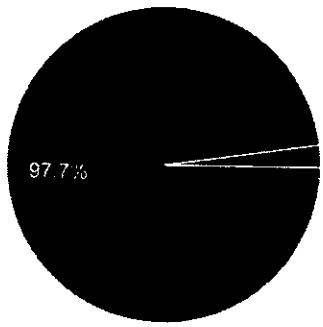
A voltage follower .....

44 responses

- has a voltage gain of 1
- is noninverting
- has no feedback resistor
- has all of these

The input stage of an Op-amp is usually a .....

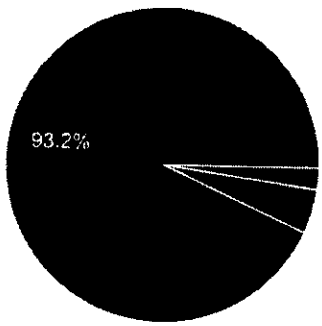
44 responses



- differential amplifier
- class B push-pull amplifier
- CE amplifier
- swamped amplifier

The binary number 10101 is equivalent to decimal number .....

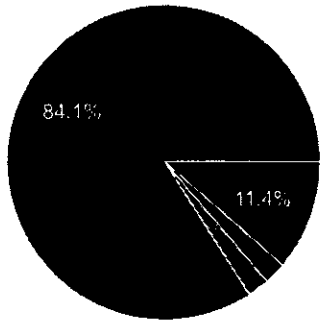
44 responses



- 19
- 12
- 27
- 21

A differential amplifier .....

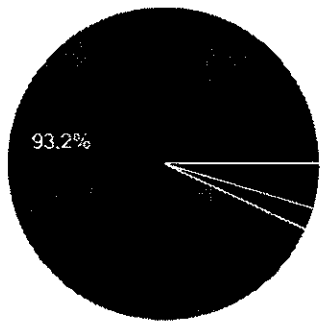
44 responses



- is a part of an Op-amp
- has one input and one output
- has two outputs
- answers (1) and (2)

In the common mode, ...

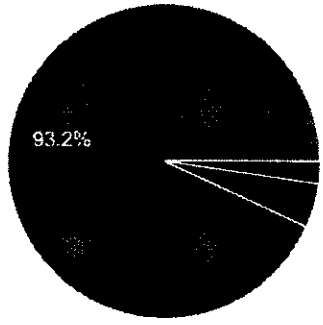
44 responses



- both inputs are grounded
- the outputs are connected together
- an identical signal appears on both the inputs
- the output signal are in-phase

With zero volts on both inputs, an OP-amp ideally should have an output .....

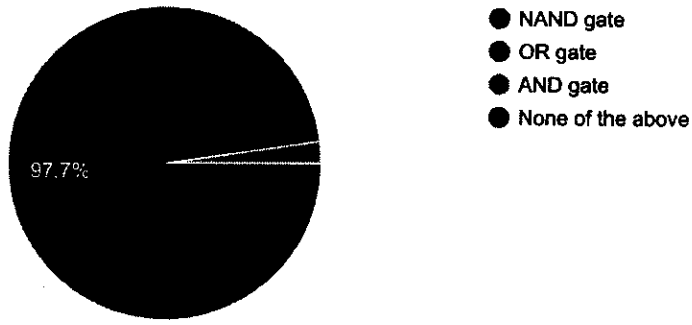
44 responses



- equal to the positive supply voltage
- equal to the negative supply voltage
- equal to zero
- equal to CMRR

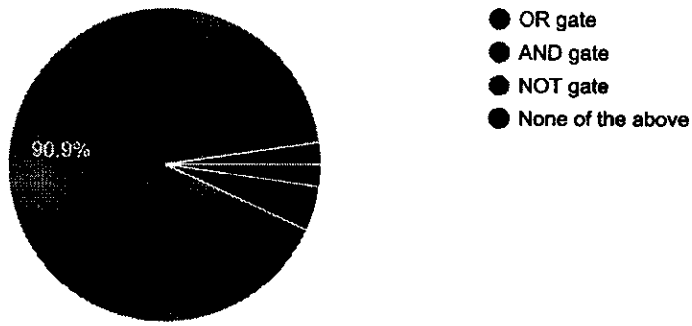
The universal gate is .....

44 responses



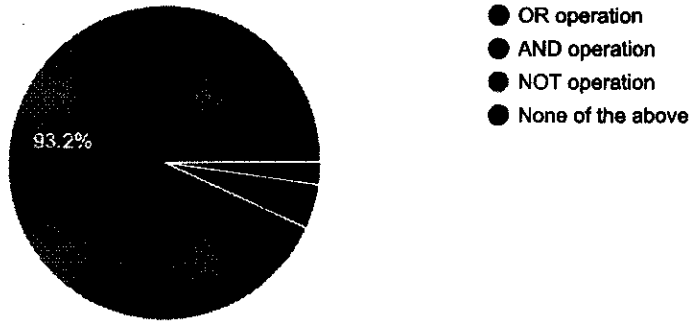
The inputs of a NAND gate are connected together. The resulting circuit is .....

44 responses



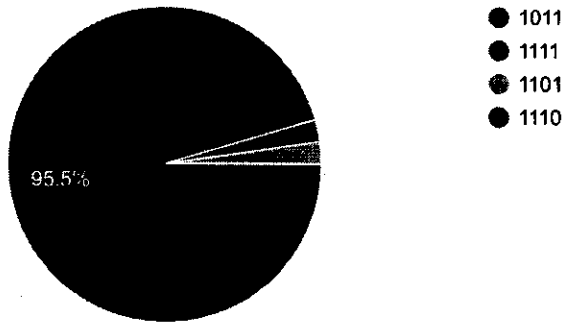
In Boolean algebra, the bar sign (-) indicates .....

44 responses



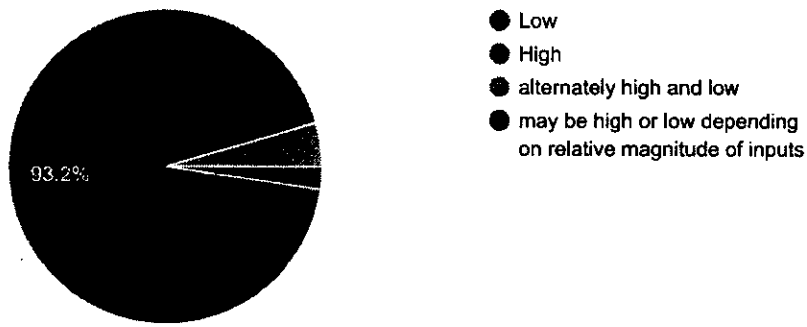
2's complement of binary number 0101 is .....

44 responses



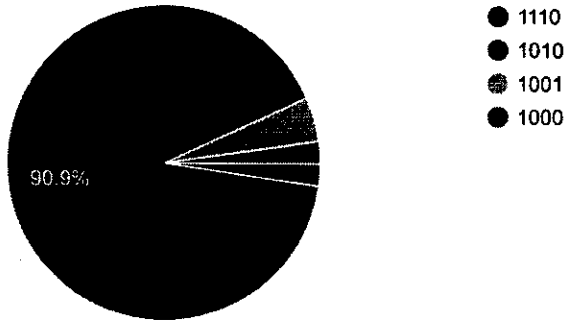
An OR gate has 4 inputs. One input is high and the other three are low. The output is .....

44 responses



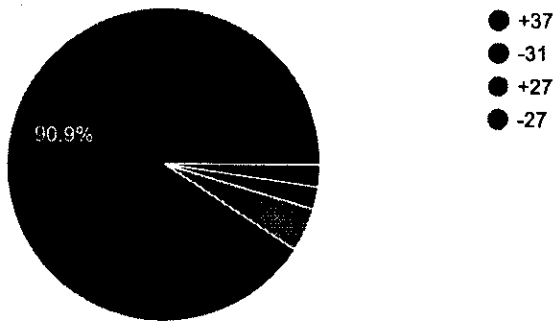
Decimal number 10 is equal to binary number .....

44 responses



In 2's complement representation the number 11100101 represents the decimal number .....

44 responses



CBCS SCHEME

USN | | | | | | | | | | |

18ELN14/24

First/Second Semester B.E. Degree Examination, Jan./Feb. 2021
Basic Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the operation of p-n junction diode under forward and reverse biased condition. **(08 Marks)**

b. Write a short note on :
i) Light emitting diode
ii) Photo coupler. **(06 Marks)**

c. Explain the operation of 7805 fixed IC voltage regulator. **(06 Marks)**

OR

2 a. With neat circuit diagram and waveform explain the working of a centre tapped full wave rectifier. **(08 Marks)**

b. Explain briefly the operation of a capacitor filter circuit. **(06 Marks)**

c. For the diode circuit shown in Fig.Q2(c), determine V_0 and I_D.

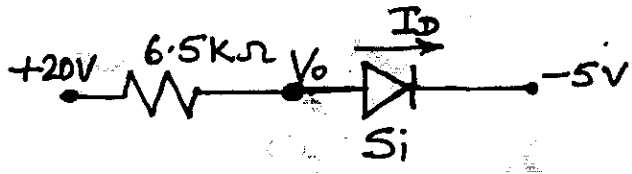


Fig.Q2(c) **(06 Marks)**

Module-2

3 a. Explain the characteristics of N-channel JFET. **(08 Marks)**

b. With neat circuit diagram, explain the working of CMOS inverter. **(08 Marks)**

c. A certain JFET has an I_{GSS} of –2nA for V_{GS} = –20V. Determine the input resistance. **(04 Marks)**

OR

4 a. Draw and explain the operations of SCR using 2 – transistor equivalent circuit. **(08 Marks)**

b. Explain phase controlled application of SCR. **(06 Marks)**

c. Explain the construction and working of P – channel enhancement type MOSFET. **(06 Marks)**

Module-3

5 a. For an op-amp :
i) List the characteristics of an ideal ap-amp
ii) Draw the three input inverting summer circuit and derive the expression for its output voltage. **(08 Marks)**

b. Define the terms :
i) Slew rate
ii) CMRR
iii) Common mode gain AC of op-amp. **(06 Marks)**

c. Design an adder circuit using an op-amp to obtain an output voltage of $-[2V_1 + 3V_2 + 5V_3]$. **(06 Marks)**

OR

6 a. Derive an expression for the output voltage of a non-inverting amplifier. **(06 Marks)**

b. With a neat diagram, explain how an op-amp can be used as a integrator. **(06 Marks)**

c. A non-inverting amplifier circuit has an input resistance of 10KΩ and feedback resistance 60Ω with load resistance of 47KΩ. Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is 1.5V. **(08 Marks)**

Module-4

7 a. Briefly explain how a transistor used as an electronic switch. **(06 Marks)**

b. Explain how 555 timer can be used as an oscillator. **(06 Marks)**

c. Define an oscillator. Derive the equation for Wien bridge oscillator. **(08 Marks)**

OR

8 a. Explain the Barkhausens criteria for oscillations. **(06 Marks)**

b. Draw and explain the operation of a voltage series feedback amplifier and derive an expression for its voltage gain with feedback. **(06 Marks)**

c. Explain the operation of an RC phase shift oscillator. **(08 Marks)**

Module-5

9 a. Convert the following :

i) $(867)_{10} = (?)_2 = (?)_{16}$

ii) $(110111101.01)_2 = (?)_{10} = (?)_{16}$. **(08 Marks)**

b. Simplify the following expressions and draw the logic circuit using basic gates.

i) $Y = \overline{AB} + \overline{AC} + A\bar{B}\bar{C} + (\overline{AB + C})$

ii) $Y = A(\overline{ABC} + A\bar{B}C)$. **(06 Marks)**

c. Realize a full adder circuit using 2 half adders. **(06 Marks)**

OR

10 a. Perform the following :

i) Convert $(ABCD)_{16} = (?)_2 = (?)_8$

ii) Convert $(4477.85)_{10} = (?)_{16} = (?)_8$. **(08 Marks)**

b. Draw and explain 4-bit shift register. **(06 Marks)**

c. With a neat block diagram, explain the working of a communication system. **(06 Marks)**

* * * * *

CBCS SCHEME

USN | | | | | | | | | | |

18ELN14/24

First/Second Semester B.E. Degree Examination, July/August 2021
Basic Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the operation of p–n junction Diode under unbiased condition with a neat diagram. **(08 Marks)**

b. In a full wave rectifier, input is from 30 – 0 – 30V. The load and R_f are 100Ω and 10Ω respectively. Calculate area voltage, efficiency, percentage regulation. **(06 Marks)**

c. Determine I_D, V_1, V_2 and V_0 for the given circuit.

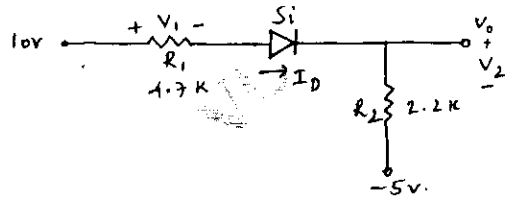


Fig.Q1(c) **(06 Marks)**

2 a. With a neat diagram and waveforms explain the working of a bridge rectifier. **(08 Marks)**

b. Explain the operation of a zener diode with line regulation and load regulation. **(08 Marks)**

c. For a zener regulator shown in Fig.Q2(c), calculate the range of input voltage for which output remain constant. $V_Z = 6.1V$, $I_{Zmin} = 2.5mA$, $I_{Zmax} = 25mA$, $r_Z = 0\Omega$.

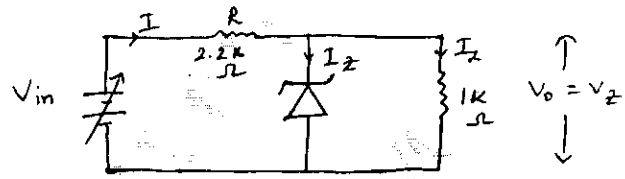


Fig.Q2(c) **(04 Marks)**

3 a. Explain the characteristics of N-channel JFET (Drawn and transfer characteristics). **(12 Marks)**

b. For a N-channel JFET, $I_{DSS} = 8mA$, $V_P = -5V$. Find :
i) I_D @ $V_{GS} = -2V$ and $-3V$
ii) V_{GS} @ $I_D = 3mA$ and $5mA$. **(06 Marks)**

c. List out classification of FET with symbols. **(02 Marks)**

4 a. Draw and explain forward and reverse characteristics of an SCR. **(07 Marks)**

b. Sketch the transfer and drain characteristics for an n-channel depletion – type MOSFET for the range of values of $V_{GS} = -6V$ to $+1V$ with $I_{DSS} = 8mA$, $V_P = V_{GS(off)} = -6V$. **(08 Marks)**

c. With a neat diagram, explain the 2 transistor model of SCR. **(05 Marks)**

5 a. Explain following with respect to OP-Amp.
i) Virtual ground ii) CMRR iii) Slew rate
iv) Offset voltage v) Matched transistors. **(10 Marks)**

b. Derive the expression for output voltage of an
i) integrator ii) inverting summing amplifier. With a neat circuit diagram. **(10 Marks)**

6 a. Explain the ideal characteristics of on op-Amp. **(08 Marks)**

b. Derive the expression for output voltage of an non inventing amplifier with a neat circuit and waveform. **(08 Marks)**

c. Design an adder circuit using an op-Amp to obtain output expression. $V_0 = -2(0.1V_1 + 0.5V_2 + 20V_3)$. **(04 Marks)**

7 a. Explain the operation of BJT as an amplifier and as a switch. **(10 Marks)**

b. Draw and explain the operation of a voltage series –ve feedback amplifier and derive an expression for its input impedance. **(10 Marks)**

8 a. Define an oscillator. Explain Brakhausen's criteria for oscillations with block diagram. **(06 Marks)**

b. Derive the expression for frequency of oscillations of Wien bridge oscillator. **(08 Marks)**

c. With a neat diagram, explain the working of RC phase shift oscillator. **(06 Marks)**

9 a. Subtract $(111001)_2$ from $(101011)_2$ using 2's complement method. **(04 Marks)**

b. State and prove Demorgan's theorem for 3 variables. **(04 Marks)**

c. Simplify the following Boolean expression :

i) $A + \overline{A}B = A + B$

ii) $\overline{X}\overline{Y}\overline{Z} + \overline{X}Y\overline{Z} + \overline{X}\overline{Y} + X\overline{Y}$

iii) $\overline{\overline{X}\overline{Y} + \overline{X}YZ + X(Y + \overline{X}\overline{Y})}$

iv) $ABC + A\overline{B}C + AB\overline{C} + \overline{A}BC$

v) $\overline{A\overline{B} + ABC + A(B + A\overline{B})}$

vi) $AB + \overline{AC} + A\overline{B}\,C(AB + C)$. **(12 Marks)**

10 a. With block diagram and truth table, explain the operation of full ladder using 2 half adder. **(08 Marks)**

b. Explain the operation NOT, AND and OR gates using analogous switch equivalent circuit. **(09 Marks)**

c. Implement Ex – OR gate using only NOR gate. **(03 Marks)**

* * * * *