V. V. Sangha's

Rao Bahadur Y. Mahabaleswarappa Engineering College

Cantonment, Ballari – 583104, Karnataka

Department of Electronics & Communication Engineering

Academic Year

2020 - 2021 (ODD ED)

Rao Bahadur Y. Mahabaleswarappa Engineering College, Ballari
Department of Electronics & Communication Engineering

COURSE FILE

Academic Year: 20 - 21 ✓ **(ODD/EVEN)**

Faculty Name	Vani. H			
Course Name	ED	EMW		
Course Code	18EC33	18ECE5		
Sem/Sec	A	B		
Verified By				

CONTENT

VISION AND MISSION OF THE INSTITUTE AND DEPARTMENT

VISION OF THE INSTITUTION

To Produce Professionally Excellent, Knowledgeable, Globally Competitive and Socially Responsible Engineers and Entrepreneurs.

MISSION OF THE INSTITUTION

M1	To Provide Quality Education in Engineering and Management.
M2	To Establish a Continuous Industry-Institute Interaction, Participation and Collaboration to Contribute Skilled Engineers.
M3	To Develop Human Values, Social Values, Entrepreneurship Skills and Professional Ethics among the Technocrats.
M4	To Focus on Innovation and Development of Technologies by Engaging in Cutting Edge Research areas.

VISION OF THE DEPARTMENT

To Produce Professionally Excellent, Knowledgeable, Globally Competitive and Socially Responsible Electronics and Communication Engineers and Entrepreneurs.

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M1	To Provide Quality Education in Electronics and Communication Engineering.
M2	To Establish a Continuous Industry-Institute Interaction, Participation and Collaboration to Contribute Skilled Electronics and Communication Engineers.
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M4	To Focus on Innovation and Development of Technologies by Engaging in Electronics and Communication Research areas.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1	Graduates of Electronics & Communication Engineering course will have successful professional career.
PEO2	Graduates of Electronics & Communication Engineering course will pursue higher education or to become an Entrepreneur.
PEO3	Graduates of Electronics & Communication Engineering course will have ability for lifelong learning and to serve the society.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO 1	Ability to Design, Develop and Test the Electronics Circuits & Communication Systems.
PSO 2	Ability to Develop Excellent Programming and Problem Solving skills in the field of Embedded System.

PROGRAM OUTCOMES (PO)

PO 1	**Engineering Knowledge**	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem Analysis**	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design/ Development of Solutions**	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems**	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage**	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and society**	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability**	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	**Individual and team work**	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication**	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance**	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning**	Recognize the need for, and have the preparation and ability to engage in Independent and life-long learning in the broadest context of technological change.

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

Name of the Staff: Mr. KHAJA MOINUDDIN, Mrs. VANI H				
Course Name: Electronic Devices				
Course Code: 18EC33	**Sem:**	**3**	**Year**	**2020-21**

COURSE OUTCOME STATEMENTS	
	At the end of the course, students will be able to ….
C203.1	Understand the principles of semiconductor physics
C203.2	Understand the principles and characteristics of different types of semiconductor devices
C203.3	Understand the fabrication process of semiconductor devices and integrated circuits
C203.4	Discuss the operation of BJT, Ebers moll coupled diode model ,cutoff , saturation and switching operation of transistor
C203.5	Understand the mathematical models of semiconductor junction and MOS transistors for circuits and systems

CO-PO/PSO Mapping

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
C203.1	3	2										2		
C203.2	3	2										2		
C203.3	3											2		
C203.4	3	2										2		
C203.5	3	2										2		
AVG	**3**	**2**										**2**		

CO	PO	Mapping	Justification
C203.1	PO1	3	The student will be able use the basic knowledge of Engineering fundamentals to understand the basics of diodes
	PO2	2	The student will be able use the knowledge of fundamentals of diode to provide solution to problem
	PO12	2	The student will be able use the knowledge of fundamentals of diode for lifelong learning
C203.2	PO1	3	The student will be able use the basic knowledge of semiconductor physics to understand principles and characteristics of different types of semiconductor devices
	PO2	2	The student will be able use the knowledge of fundamentals of different types of semiconductor devices to provide solution to problem
	PO12	2	The student uses the knowledge of different types of semiconductor devices for lifelong learning
C203.3	PO1	3	The student uses the knowledge of engineering fundamentals to understand fabrication process of semiconductor devices
	PO12	2	The student uses the knowledge of fabrication process of semiconductor devices for lifelong learning
C203.4	PO1	3	The student uses the engineering knowledge to understand mathematical models of transistor,switching operation of transistor
	PO2	2	Students will be able to solve problems on amplification of transistor
	PO12	2	The student uses the knowledge of mathematical models of mathematical models of transistor,switching operation of transistor for designing of amplifiers and switching circuits as lifelong learning
C203.5	PO1	3	The student uses the engineering knowledge to understand mathematical models of semiconductor junction and MOS transistors for circuits and systems
	PO2	2	Students will be able to solve problems on MOSFETs
	PO12	2	The student uses the knowledge of mathematical models of semiconductor junction and MOS transistors for lifelong learning

Course Coordinator

Staff Signature

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

CO Analysis

Name of the Staff: Mr. KHAJA MOINUDDIN, Mrs VANI H				
Course Name: Electronic Devices				
Course Code: 18EC33	Sem:	3	Year	2020-21

CO	Description
C203.1	Explain the principles of semiconductor physics **Action:** Explain **Knowledge:** principles of semiconductor physics **Condition:** None **Criterion:** None
C203.2	Explain the principles and characteristics of different types of semiconductor devices. **Action:**Explain **Knowledge:**principles and characteristics Programming language basics **Condition**: None **Criterion:**different types of semiconductor devices.
C203.3	Summarize the fabrication process of semiconductor devices **Action:** Summarize **Knowledge:**fabrication process **Condition:** None **Criterion:** of semiconductor devices
C203.4	Discuss the operation of BJT, Ebers moll coupled diode model ,cutoff , saturation and switching operation of transistor **Action:** Discuss **Knowledge:**Discuss the operation of BJT, Ebers moll coupled diode model ,cutoff , saturation and switching operation of transistor **Condition:** None **Criterion:**None
C203.5	Describe the mathematical models of semiconductor junction and MOS transistors for circuits and systems **Action:**Describe **Knowledge:**mathematical models of semiconductor junction and MOS transistors **Condition:** None **Criterion:**for circuits and systems

Staff signature

Tentative Academic Calendar of VTU, Belagavi for ODD Semester of 2020-2021

	I Sem B. E. / B. Tech. / B. Arch./B.Plan	I sem M.Tech./MBA /MCA/M.Arch.	III, V & VII Sem B. E. /B. Tech./B.Plan/ B.Arch & IX Sem B. Arch.	III & V Sem MCA	III Sem MBA	III Sem M, Tech.	III Sem M. Arch.
Commencement of ODD Semester	Will be announced later	Will be announced later	01.09.2020	01.09.2020	01.09.2020	01.09.2020	01.09.2020
Last Working day of ODD Semester			17.12.2020	17.12.2020	17.12.2020	17.12.2020	17.12.2020
Practical Examinations			21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020
Theory Examinations			04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021
Internship Viva-Voce			-	-	-	**25.01.2021 To 08.02.2021**	-
Professional training / Organization study			-	-	-		-
Commencement of EVEN Semester			08.02.2021	08.02.2021	08.02.2021	22.02.2021	08.02.2021

NOTE

- VII Semester B. E / B. Tech students shall have to undergo INTERNSHIP as per circular of University **VTU/Aca/2019-20/85, dated 12.05.2020**.
- I Semester B. E/ B. Tech / B. Arch Students shall compulsorily undergo Induction Program for a period of 3 Weeks as per the schedule given by VTU Belagavi
- The classroom sessions for all the higher semesters would be commencing from 01.09.2020(Tentative) in ONLINE mode until further orders.
- The Institute needs to function for six days a week with additional hours.
- The faculty/staff shall be available to undertake any work assigned by the university.
- If any of the above date is declared to be a holiday then the corresponding event will come into effect on the next working day.
- Notification regarding Calendar of Events relating to the conduct of University Examinations will be issued by the Registrar (Evaluation) from time to time.
- **Academic Calendar may be modified based on guidelines/directions issued in future by MHRD/UGC/AICTE/State Government.**

12.9.2020.

REGISTRAR

V.V. Sangha's
ರಾವ್ ಬಹದ್ದೂರ್ ವೈ. ಮಹಾಬಲೇಶ್ವರಪ್ಪ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜ್, ಬಳ್ಳಾರಿ
Rao Bahadur Y. Mahabaleswarappa Engineering College, Ballari
Cantonment, Ballari-583104. Tel: 08392-244809. Fax: 08392-242148

ACADEMIC CALENDAR 2020-21 (ODD SEM)

MONTH	DAY	DATE	EVENT	DESCRIPTION
September	Tuesday	01-09-2020	Commencement of ODD Semester	UG:-III,V,VII Sem Commencement of Classes.
	Tuesday	01-09-2020		PG:- III Sem Commencement of Classes.
	Monday	07-09-2020	Submission of Workload	Submit Final Faculty Teaching Workload.
	Saturday	19-09-2020	Parents Meet	Parents Meet should be arranged only for 3rd & 5th Sem Students
	Monday	21-09-2020	Course File Verification	Verification of Course plan & CO,PO Mapping
October	Saturday	17-10-2020		
	Sunday	18-10-2020	I-Internal Assessment Test	Prepare I IA Question Paper as Per VTU Pattern
	Monday	19-10-2020		
	Saturday	24/10/2020	Submit I-IA Marks	Enter I-IA Marks in RYMEC Online Portal on or Before said Date.
	Tuesday	27/10/2020	IA Reports to Parents	Dispatch of I-IA Marks , Attendance % through SMS to Parents on or Before said Date.
	Wednesday	28/10/2019	First Assignment Submission	Student should submit 1st Assignment on or before said date.
	Thursday	29/10/2020	Interaction with Parents	Interaction with Parents & Students Performance Review
November	Monday	02-11-2020	Verifying the Course file	Verifying the Assessment Strategies
	Wednesday	20-11-2020		
	Thursday	21-11-2020	II-Internal Assessment Test	Prepare II IA Question Paper as Per VTU Pattern
	Friday	22-11-2020		
	Wednesday	25-11-2020	Submit II-IA Marks	Enter II-IA Marks in RYMEC Online Portal Before said Date.
	Saturday	26-11-2020	IA Reports to Parents	Dispatch of II-IA Marks , Attendance % through SMS to Parents on or Before said Date.
	Monday	27-11-2020	First Assignment Submission	Student should submit 2nd Assignment on or before said date.
December	Saturday	05-12-2020	Interaction with Parents	Interaction with Parents & Students Performance Review
	Monday	07-12-2020	Verifying the Course file	Verifying the Assessment Strategies
	Friday	14-12-2020		
	Saturday	15-12-2020	III-Internal Assessment Test	Prepare IIIA Question Paper as Per VTU Pattern
	Sunday	16-12-2020		
	Wednesday	18/12/2020	Submit III-IA Marks	Enter III-IA Marks in RYMEC Online Portal Before said Date.
	Thursday	19/12/2020	IA Reports to Parents	Dispatch of III-IA Marks, Attendance % & Final Average Marks through SMS to Parents on or Before said Date.
	Thursday	17-12-2020	Last Working Day of Odd Sem 2020-21	UG:-III,V,VII Sem Last Working Day
	Thursday	17-12-2020		PG:- III Sem Last Working Day

RaoBahadur Y Mahabaleswarappa Engineering College, Ballari
Department of Electronics and Communication Engineering

Academic Calendar of Events
ODD Semester 2020-21(SEP 2020-March 2021)

	III, V& VII Sem B.E/B.Tech	III Sem M.Tech
Pre Placement Training	For VI Semester Students of all Branches from 20th to 25th Sep2020	
Commencement of ODD Semester	1st SEP 2020	
Admission Publicity in and around Ballari	SEP & OCT 2020	
I Internal Assessment Test	17th, 18th & 19th OCT 2020 (Sat, Sun & Mon-Online)	
One day Online FDP on **"Virtual Lab"** organized by VTU in collaboration with NITKSuratkal by Dr. K.V. Gangadharan	21st OCT 2020	
Last date for sending IA Marks (SMS)	27th OCT 2020	
Parents Meet	29th OCT 20220	
II Internal Assessment Test	1st, 2nd & 3rd DEC 2020 (Tue, Wed & Thu-Online)	
Last date for sending IA Marks (SMS)	6th DEC 2020	
Parents Meet	9th DEC 2020	
Fresher's Day & First Year Student Induction Programme through Digital Platform	17th DEC 2020	
Student Induction Programme **UHV Session-2** through Digital Platform for 1st Year Students	19th DEC 2020	
One day Seminar On **"FUTURE READY: Industry 4.0"** by Mr. MKHH Jilani, Investment banker & Strategic advisor, KBN, university.	23rd DEC 2020	
III Internal Assessment Test	11th,12th &13th JAN 2021(Thu, Fri & Sat-Offline)	
Webinar on **Introduction to Remote Sensing & Image Processing by** Dr. P. M Shivakumar Swamy Professor, JSSTE, Bangalore	12th JAN 2021	
Last date for sending IA Marks (SMS)	23rd JAN 2021	
PG **Freshers's Day & Inaugural** Function	23rd JAN 2021	
Parents Meet	25th JAN 2021	
Webinar on **Interpersonal Skills** by Ms. Sonu Prakash Chand, Manager IT Solutions, Eli Lily & Company	25th JAN 2021	
Quiz on **Intellectual Property Rights**	27th JAN 2021	
External NBA Audit By on Mrs. Sowmyashree M.S, BMSIT, Bengaluru	29th JAN 2021	
Internal NBA Audit	19th FEB 2021	
IEEE VTools webinar titled **"Automation in Electronics Engineering"** jointly organized by IEEE Bangalore Section, RYMEC Ballari, by Ramachandra Gambheer Member of IEEE, Western USA	28th FEB 2021	
Webinar on **"Academic and Administrative Audit Process "** under EDP in association with IQAC	4th March 2021	

Dr. T. Hanumantha Reddy & Dr. Veeragangadhar Swamy .		
External Academic Audit (IQAC-NAAC) Dr. Prakash M Prof, SDM Engineering College, Dharwad	6th MARCH 2021	
Last Working Day	**16/01/2021**	
Practical Examination	21/01/2021 to 02/02/2021	21/01/2021 to 27/01/2021
Theory Examination	08/02/2021 to 25/03/2021	28/01/2021 to 10/02/2021
Commencement of EVEN Semester	**19/04/2021**	19/02/2021

HOD ECE

Head of the Department
Electronics & Communication Engg
R. Y. M. Engineering College,
(Formerly Vijayanagar Engg. College)
BELLARY-583 104

V.V.Sangha's

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics & Communication Engineering

Time Table

Staff Name: Vani. H	**Sem :** 3 **Sec:** A
Course Name: Electronic Devices	**Course Code:** 18EC33
Lab Name: ED & I lab	**Code:** 18ECL37

Day	9am-9:55am	9:55am-10:50am	10:50am-11:00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
Monday			BREAK			BREAK			
Tuesday									
Wednesday	ED								
Thursday		ED							
Friday					ED				
Saturday									

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

COURSE PLAN 2020-21 (ODD SEM)

Staff Name:Khaja Moinuddin/ Vani H	**Course Type: Core/ Elective(Open/Professional)**	**Sem / Sec: 3rd A/B**
Course Name: Electronic Devices	**Course Code: 18EC33**	**Total Number of Lecture Hours:40**
Max marks: 100	**Prerequisites: Basic Electronics**	

Sl.No	Module Name	Lecture Hours Required
01	**Semiconductors**	**8**
02	**P-N Junctions**	**8**
03	**Bipolar Junction Transistors**	**8**
04	**Field effect Transistors**	**8**
05	**Fabrication of P-N junction and Integrated Circuits**	**8**

Sl.No	Date	Time	Topic to be Covered
1	2-9-2020	9.30-10.30	**Semiconductor Devices**: Introduction, Energy bands
2	3-9-2020	11-12	Bonding forces in solids, Metals, Semiconductors and Insulators
3	4-9-2020	2.30-3.30	Direct and Indirect semiconductors, Electrons and Holes
4	9-9-2020	9.30-10.30	Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance
5	10-9-2020	11-12	Effects of temperature and doping on mobility
6	16-9-2020	9.30-10.30	Hall Effect
7	18-9-2020	2.30-3.30	Continued
8	23-9-2020	9.30-10.30	**P-N Junctions** Introduction, Forward and Reverse biased junctions
9	24-9-2020	2.30-3.30	Qualitative description of Current flow at a junction, reverse bias
10	25-9-2020	2.30-3.30	Reverse bias breakdown, Zener breakdown, avalanche breakdown
11	30-9-2020	9.30-10.30	Rectifiers.
12	1-10-2020	11-12	Optoelectronic Devices Photodiodes
13	7-10-2020	9.30-10.30	Current and Voltage in an Illuminated Junction
14	8-10-2020	11-12	Photo detectors.
15	9-10-2020	11-12	Light Emitting Diode:

16	14-10-2020	9.30-10.30	Light Emitting materials
17	15-10-2020	11-12	**Fundamentals of BJT operation** Amplification with BJTS,
18	21-10-2020	11-12	BJT Fabrication
19	22-10-2020	3.30-4.30	BJT Fabrication
20	27-10-2020	11-12	The coupled Diode model (Ebers-Moll Model),
21	29-10-2020	9.30-10.30	The coupled Diode model (Ebers-Moll Model),
22	29-10-2020	11-12	Switching operation of a transistor, Cutoff, saturation, specification
23	19-11-2020	2.30-3.30	Drift in the base region, Base narrowing
24	20-11-2020	2.30-3.30	switching cycle.
25	21-11-2020	2.30-3.30	**Basic pn JFET Operation**
26	25-11-2020	9.30-10.30	Equivalent Circuit and Frequency Limitations
27	27-11-2020	2.30-3.30	Energy band diagram
28	4-12-2020	9.30-10.30	Ideal Capacitance – Voltage Characteristics and Frequency Effects
29	5-12-2020	11-12	Ideal Capacitance – Voltage Characteristics and Frequency Effects
30	11-12-2020	9.30-10.30	MOSFET- Two terminal MOS structure
31	12-12-2020	11-12	Basic MOSFET Operation- MOSFET structure
32	17-12-2020	9.30-10.30	Current-Voltage Characteristics
33	21-12-2020	04.05-5.00	Current-Voltage Characteristics
34	26-12-2020	3.10-4.05	**Fabrication of p-n junctions**
35	28-12-2020	04.05-5.00	Thermal Oxidation
36	28-12-2020	3.10-4.05	Diffusion, Rapid Thermal Processing
37	1-1-2021	2.15-3.10	Ion implantation
38	4-1-2021	04.05-5.00	chemical vapour deposition
39	8-1-2021	2.15-3.10	photolithography

40	15-1-2021	2.15-3.10	Etching, metallization
41	16-1-2021	11-12	**Integrated Circuits** : Background, Evolution of ICs
42	18-1-2021	04.05-5.00	CMOS Process Integration
43	19-1-2021	2.15-3.10	CMOS Process Integration
44	20-1-2021	2.15-3.10	CMOS Process Integration
45	21-1-2021	11-12	Integration of Other Circuit Elements.
46	23-1-2021	11-12	Integration of Other Circuit Elements.

Teaching and Learning Tools: Blackboard/PowerPoint presentation/webinar/lab.

Text Books:

Ben.G.Streetman, Sanjay Kumar Banergee, "Solid State Electronic Devices" &th Edition, Pearson Edition,2016, ISBN 978-93-325-5508-2.

Donald A Neamen, Dhrubes Biswas, "Semiconductor physics and Devices", 4th edition, MCGraw Hill Education, 2012, ISBN 978-0-07-107010-2.

Reference Books:

SM Sze, Kwok K.Ng, "Physics of Semiconductor Devices," 3rd edition, Wiley, 2018

A Bar-Lew, "Semiconductor and Electronic Devices", 3rd edition, PHI, 1993

Innovative Practices:

1. Quiz Test
2. Problem Solving Skill Development

Staff Signature

HOD

Rao Bahadur .Y. Mahabaleshwarappa Engineering College Bellary

Dept ECE	2020 - 2021	Title: Report on Syllabus Status

REPORT ON SYLLABUS STATUS

Semester	Branch	Subject	Section	Name of the Staff
3	ECE	EA	A & B	Khaja Moinuddin / Vani. A.

Sl.No	Date	Period	Topics Covered	Remarks
1	2/9/20	9:30-10:30	Semiconductor Devices: Introduction, Energy bands	
2	3/9/20	11-12	Bonding force in solids, Metals, Semiconductors and insulators	
3	4/9/20	2:30-3:30	Direct & indirect S.C, electrons & Holes	
4	9/9/20	9:30-10:30	Intrinsic & extrinsic materials conductivity & mobility drift & resistance	
5	10/9/20	11-12	Effects of temp and doping on mobility	
6	16/9/20	9:30-10:30	Hall effect	
7	18/9/20	2:30-3:30	Continued	
8	23/9/20	9:30-10:30	P-N Junctions	
9	24/9/20	2:30-3:30	Qualitative description of current flow at a junction reverse bias	
10	25/9/20	2:30-3:30	Reverse bias breakdown, zener breakdown avalanche breakdown	
11	30/9/20	9:30-10:30	Rectifiers	
12	1/10/20	11-12	opto electronic devices, Photodiodes	
13	7/10/20	9:30-10:30	Current & voltage in an illuminated jnc	
14	8/10/20	11-12	Photo detectors	
15	9/10/20	11-12	Light Emitting Diode	
16	14/10/20	9:30-10:30	Light emitting materials	
17	15/10/20	11-12	Fundametals of BJT, amplication	
18	21/10/20	11-12	BJT fabrication	
19	22/10/20	3:30-4:30	BJT fabrication	
20	27/10/20	11-12	The coupled Diode Model (Ebers Moll Model)	
21	29/10/20	9:30-10:30	The coupled Diode Model (Ebers-Moll model)	
22	29/10/20	11-12	switching operation of transistor, cutoff, saturation amplification	
23	19/11/20	2:30-3:30	Drift in the base region, Base narrowing	
24	20/11/20	2:30-3:30	switching cycle	
25	21/11/20	2:30-3:30	Basic PN JFET operation	
26	25/11/20	9.30-10:30	Equivalent circuit and frequency limitations	
27	27/11/20	2.30-3.30	Energy band diagram	
28	4/12/20	9:30-10:30	Ideal capacitance - voltage characteristics & frequency effects	
29	5/12/20	11-12	Ideal capacitance - voltage characteristics and frequency effects	

Signature
Staff In-charge

Name of the staff Vani. H

Signature
Head of the Department

Rao Bahadur .Y. Mahabaleshwarappa Engineering College Bellary

Dept ECE	2020 -- 2021	Title: Report on Syllabus Status

REPORT ON SYLLABUS STATUS

Semester	Branch	Subject	Section	Name of the Staff
3	ECE	ED	A & B	KHaja Moinuddin / Vani. H.

Sl.No	Date	Period	Topics Covered	Remarks
30	11/12/2020	9:30-10:30	MOSFET - two terminal MOS structure	
31	12/12/20	11-12	Basic MOSFET operation - MOSFET structure	
32	17/12/20	9:30-10:30	Equivalent circuits & frequency	
33	21/12/20	4:05-5:00	Current - voltage characteristics	
34	26/12/20	3:10-4:05	Fabrication of P-N junction	
35	28/12/20	4.05-5.00	Thermal oxidation	
36	28/12/20	3:10-4.05	Diffusion, Rapid Thermal Processing	
37	1/1/21	2:15-3:10	Ion implantation	
38	4/1/21	4:05-5:00	chemical vapour deposition	
39	8/1/21	2:15-3.10	Photolithography	
40	15/1/2021	2:15-3:10	Etching, metallization	
41	16/1/2021	11-12	Integrated circuits:- Background, Evolution ICs	
42	18/1/2021	4:05-5:00	CMOS process Integration	
43	19/1/2021	2:15-3:10	CMOS process Integration	
44	20/1/2021	2:15-3:10	CMOS process Integration	
45	21/1/2021	11-12	Integration of other circuit element	
46	23/1/2021	11-12	Integration of other circuit element	

Signature
Staff In-charge

Name of the Staff Vani. H

Signature
Head of the Department

COURSE EVALUATION AND ASSESSMENT SCHEME 2018

	What		To Whom	When/ Where (Frequency in the course)	Max Marks	Evidence Collected
Direct Assessment Methods	IA	Internal Assessment Tests	Students	Thrice(Average of three IA Tests)	30	Blue Books
		Assignment		Thrice(Before IA Test and average of 3 is taken)	10	Assignment Books
		Practical Assessment		Once	40	Practical evaluation
	FE	Final Examination		End of Course (Answering One of two questions from five Modules	100	Result sheet
		Practical Examination		One question from lot	100	Result sheet
Indirect Assessment Methods	Students Feedback		Students	End of the course	-	Questionnaire
	Course Exit Survey					

Questions for IA and FE will be designed to evaluate the various educational components (Bloom's taxonomy)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
CONTINIOUS INTERNAL EVALUATION-I (20-21 Odd Sem)

Staff Name: Mr. Khaja Moinuddin / Mrs Vani H	**Sem: III** A /B	**Date:** 18/10/2020
Course Name: Electronic Devices	**Course Code:**18EC33	**Time :9.15-10.45AM**
Max marks: 50	**Prerequisites:** Basic Electronics	**Total Contact Hours :** 40

NOTE: Answer five questions (at least one from each pair of questions)

Q No	QUESTIONS	Marks	BTL	CO	PO	PSO
Q1	Explain different types of bonding forces in solids	10	L2	1	1	
	OR					
Q2	Develop the equation for mobility of electron and holes ,current density in terms of conductivity	10	L2	1	1	
Q3	Explain extrinsic semiconductors with energy band diagram marking donor and acceptor energy level	10	L2	1	1	
	OR					
Q4	a)Classify metals, semiconductors and insulator with energy band diagram b)Explain direct and indirect semiconductors	6 4	L2 L2	1	1	
Q5	Explain i)Lattice scattering ii) Impurity scattering	10	L2	1	1	
	OR					
Q6	Explain Hall effect with neat diagram and necessary equations	10	L2	1	1	
Q7	Explain a) Zener breakdown b) Avalanche breakdown	10	L2	2	1	
	OR					
Q8	Explain flow of current in forward biased and reverse biased PN junction with diagrams	10	L2	2	1	
Q9	Explain formation of conduction and valence band when N atoms of silicon comes closer to form crystalline structure with diagram	10	L2	1	1	
	OR					
Q10	a) Explain how electron hole pairs are created b) discuss drift of charge carriers in semiconductor with diagram	5 5	L2	1	1	

IA Co-ordinator

Signature of faculty

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SCHEME OF EVALUATION CIE-III (20-21 Odd Sem)

Staff Name: Mr. Khaja Moinuddin / Mrs Vani H	**Sem:** III A /B	**Date:** 13/01/2021
Course Name: Electronic Devices	**Course Code:**18EC33	**Time :**9.15-10.45AM
Max marks: 50	**Prerequisites:** Basic Electronics	**Total Contact Hours :** 40

Q1)

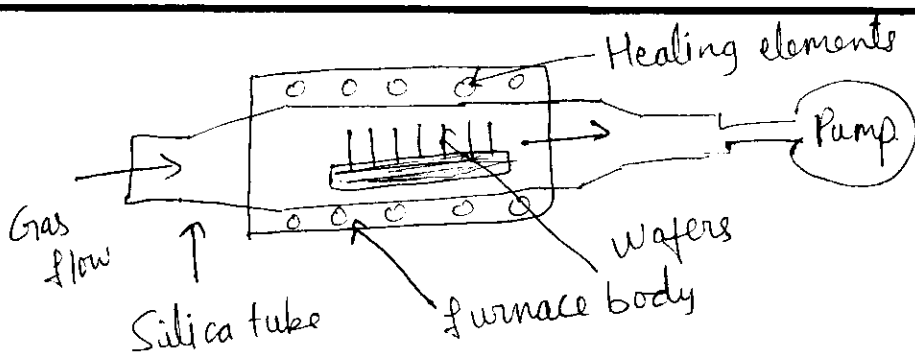
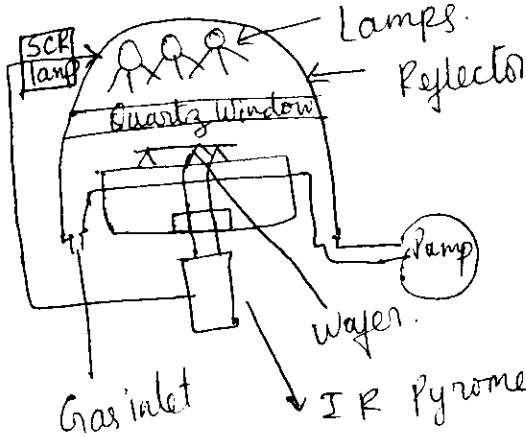


figure (5M)
Explaination (5M)

2)



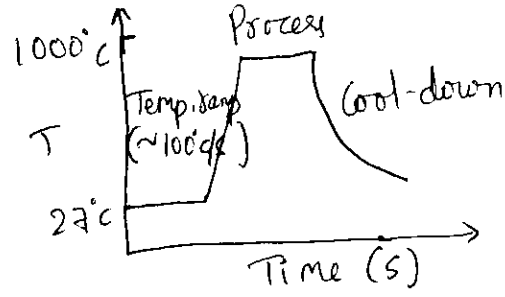


figure (5M)
Explaination (5M)

3) Photolithography
figure (5M) Explaination (5M)

4) Thermal Oxidation

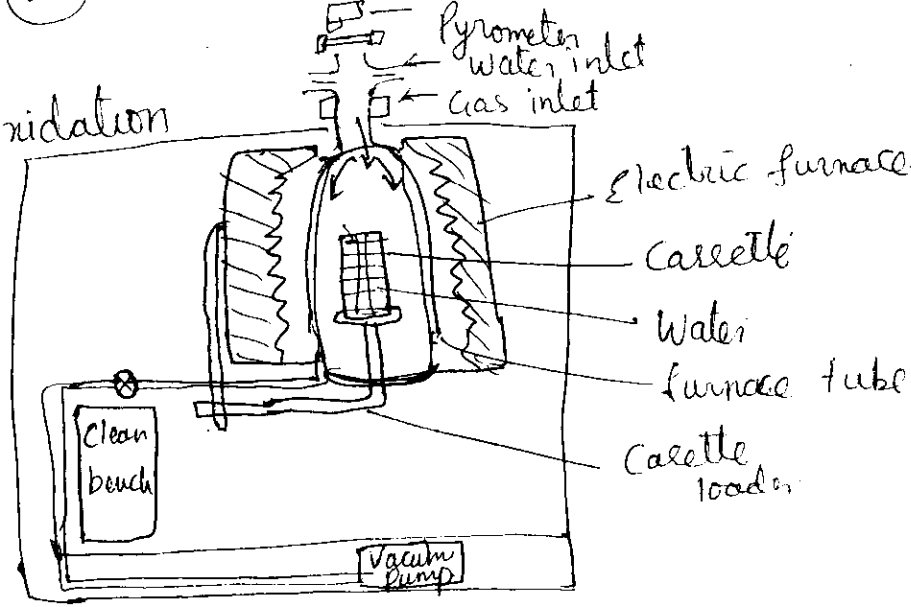


figure (5M)
Explaination (5M)

5)

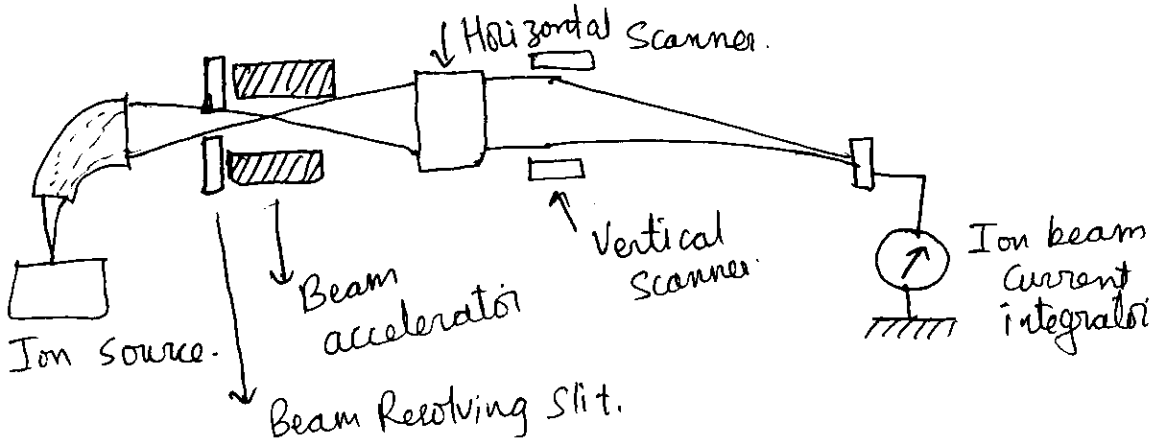
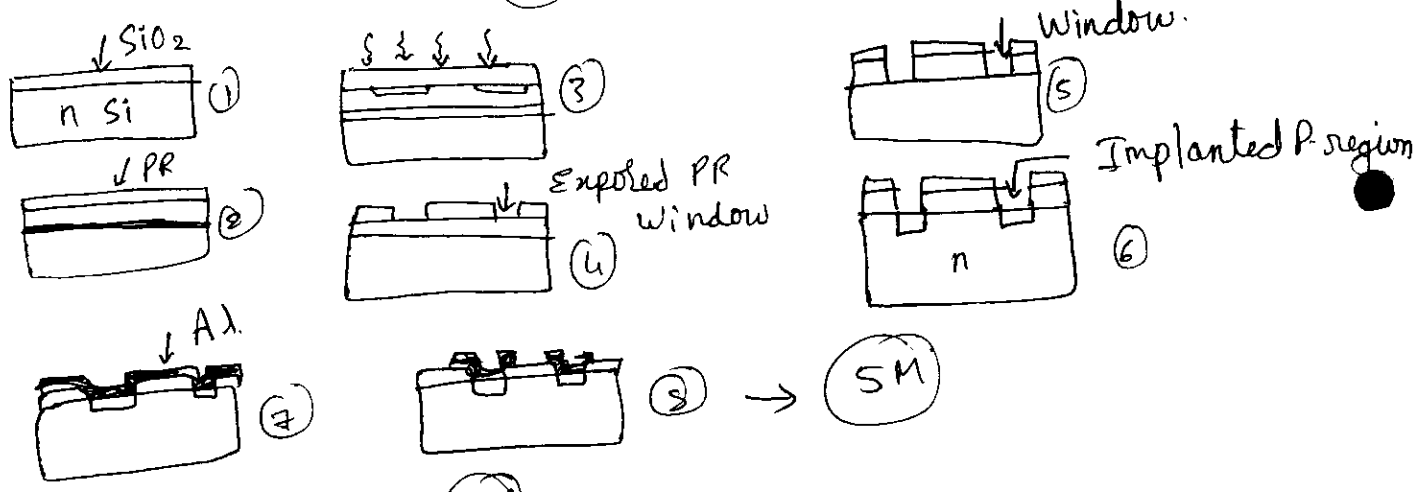


Figure (5M)

Explaination (5M).

6)



(1) (2) (3) (4) (5) (6) (7) (8) → (5M)

Explaination (5M).

7) Solar cell

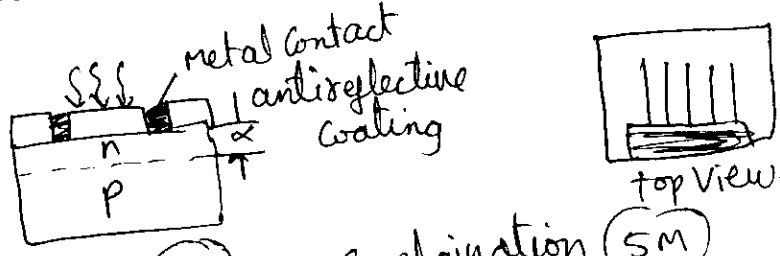
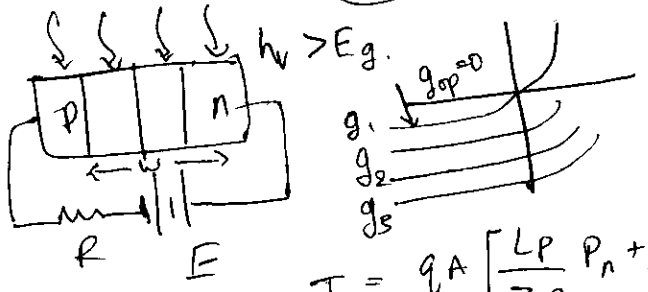


figure (3M) Explaination (5M).

8)



— (2M)

Explaination (3M).

$$I = qA\left[\frac{L_p}{z_p}P_n + \frac{L_n}{z_n}n_p\right]\left(e^{qV/KT} - 1\right) - qA g_{op}\left(L_p + L_n + w\right).$$

$V = 0$.

$I = -I_{op}$ Short circuit current — (3M).

Open Ckt V/g $I = 0$. $V_{oc} = \frac{KT}{q}\ln\left[\frac{g_{op}}{g_{pn}}\right]$ — (2M)

9) a) Classification (4M). (b) List — (2M) advantages explanation (4M)

10) figure (5M) CMOS Process Integration

Explanation (5M)

IA-1 PERFORMANCE ANALYSIS

Internal Assessment 1

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
CO mapping	CO1	CO1	CO1	CO1	CO1	CO1	CO2	CO2	CO1	CO1
Max Marks /Question	10	10	10	10	10	10	10	10	10	10
Total marks of class /question	340	-	20	315	120	214	311	-	165	145
No. of students attended	34	-	2	32	12	23	33	-	18	15
No of students scored > 65% of marks/Question	34	-	2	31	12	20	30	-	15	14
Percentage of students scored>65% of marks/Question	100.00	-	100.00	96.88	100.00	86.96	90.91	-	83.34	93.34

Mark range	0-10	11 to 20	21 to 30	31-40	41-50
No. Of Students	0	0	0	0	33

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics and Communication Engineering

CONTINUOUS INTERNAL EVALUATION ASSESSMENT REPORT

Staff Name: Mr. Khaja Moinuddin/ Mrs Vani H **Sem/Sec:** 3/A&B **Academic year:** 20-21

Course Name: ED **Course code:** 18EC33 **CIE:** 1

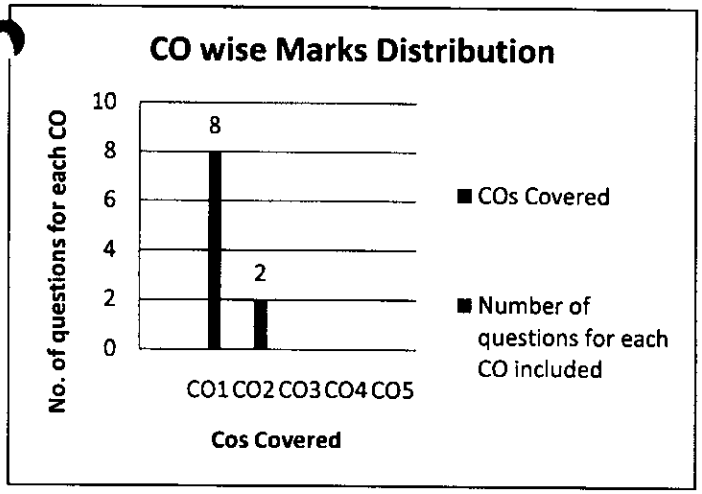
Mention the Syllabus included for CIE:

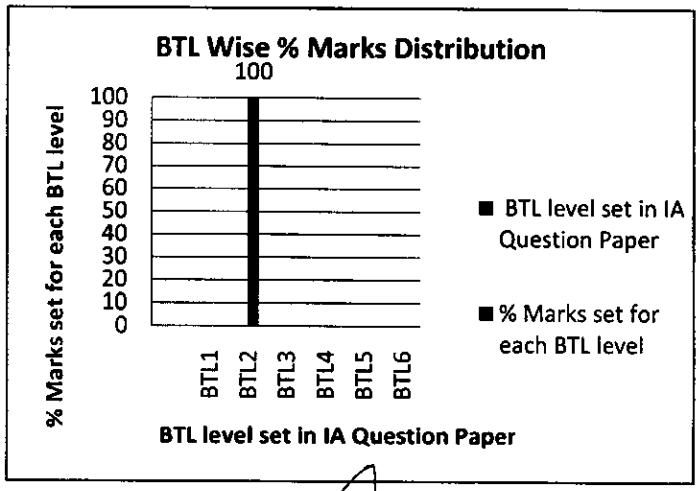
1	MODULE NUMBERS	1,2
2	CO s COVERED	CO1,CO2
3	BTL LEVELS ADDRESSED	L2

Mention following details of CIE Questions Paper setting :

1	COs Covered	CO1	CO2	CO3	CO4	CO5
		Y	Y			
2	Number of questions for each CO	8	2			

1	BTL level set in IA Question Paper	BTL1	BTL2	BTL3	BTL4	BTL5	BTL6
			Y				
2	% Marks set for each BTL level		100				





Staff Signature

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CONTINIOUS INTERNAL EVALUATION-II (20-21 Odd Sem)

Staff Name: Mr. Khaja Moinuddin / Mrs Vani H	**Sem: III** A /B	**Date:** 02/12/2020
Course Name: Electronic Devices	**Course Code:**18EC33	**Time :2.30-4.00PM**
Max marks: 50	**Prerequisites:** Basic Electronics	**Total Contact Hours :** 40

NOTE: Answer five questions (at least one from each pair of questions)

Q No	QUESTIONS	Marks	BTL	CO	PO	PSO
Q1	Explain Operation of N-channel JFET with diagrams	10	L2	5	1	
	OR					
Q2	Explain Operation of N-channel Enhancement MOSFET with diagrams	10	L2	5	1	
Q3	Explain ideal C-V characteristics with necessary equations and diagram	10	L2	5	1	
	OR					
Q4	Discuss energy band diagram for p-channel MOS capacitor with positive and negative bias voltage	10	L2	5	1	
Q5	Explain small signal equivalent circuit with necessary equations	10	L2	5	2	
	OR					
Q6	a)Explain pnp transistor in common base configuration mentioning requirement of good transistor	10	L2	4	1	
Q7	Explain how transistor works as an amplifier with all necessary factors equation and diagrams	10	L2	4	1	
	OR					
Q8	a)Sketch the diagram showing hole and electron flow in pnp transistor and explain b) Compute I_B and I_C assume τ_p=10μs τ_t=0.1μs R_B=50KΩ V_{BB}=5V	6 4	L3	4	2	
Q9	Discuss the concept of drift in base region with diagram and necessary equations	10	L2	4	1	
	OR					
Q10	a)Explain switching operation for transistor in common emitter configuration b)Define i)Rise time(tr) ii)Fall Time(tf)	6 4	L2 L1	4	2	

IA Co-ordinator **Signature of faculty**

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SCHEME OF EVALUATION-II (20-21 Odd Sem)

Staff Name: Mr. Khaja Moinuddin / Mrs Vani H	**Sem:** III A /B	**Date:** 02/12/2020
Course Name: Electronic Devices	**Course Code:** 18EC33	**Time :2.30-03.45PM**
Max marks: 50	**Prerequisites:** Basic Electronics	**Total Contact Hours :** 40

Q1) Operation of JFET.
→ Cross Section View of n-Channel JFET — (2M)
→ Gate to Channel Space Charge regions & I-V Characteristics @ zero V_{ch}, Small reverse biased gate V/g & a gate Voltage to achieve Pinch off — (4M)
→ Gate to Channel Space Charge regions I-V Characteristics @ zero V_{ch} & Small drain V/g. larger drain V/g & a drain V/g to achieve Pinch off at drain terminal

Q2) N-Channel MOSFET Operation
necessary diagram for n-Channel MOSFET — (10M)
C-V Characters

Q3) C-V Characteristics with necessary equations — (5M)
necessary diagrams — (5M)

Q4) Energy band diagram for p-channel MOSFET
necessary [illegible] MOS Capacitor with an n-type substrate
for i) positive gate bias ii) Moderate negative gate bias (10M)

Q5) Small Signal equivalent circuit

All necessary figures ⇒ Cross section of JFET with γ_s & γ_d.
⇒ Small Signal equivalent ckt of JFET.
⇒ Ideal low-frequency Small Signal ckt
⇒ Ideal equivalent ckt including γ_s.

$I_{ds} = g_m V_{gs}$ $\quad V_{gs} = V_{g's'} + (g_m V_{g's'})\gamma_s = (1 + g_m\gamma_s) V_{g's'}$

$I_{ds} = g_m V_{g's'}$ $\quad I_{ds} = \left(\frac{g_m}{1 + g_m\gamma_s}\right) V_{gs} = g_m' V_{gs}$ — (10M)

Q6) PNP transistor in CB Configuration — (6M)
Requirements of good transistor — (4M)

Q7) Transistor as an amplifier with necessary factors and diagrams — (10M)

Q8) a) Electron hole flow diagram — (5M)

b) $I_B = 0.1\,mA$
$I_C = 10\,mA$ — (5M)

Q9) Drift in base region.

$$I_n(x_n) = qA\mu_n N(x_n)\mathcal{E}(x_n) + qAD_n\frac{dN(x_n)}{dx_n} = 0$$

$$\mathcal{E}(x_n) = -\frac{D_n}{\mu_n}\frac{1}{N(x_n)}\frac{dN(x_n)}{dx_n} = \frac{KT}{q}\frac{1}{N(x_n)}\frac{dN(x_n)}{dx_n}$$ — (5M)

Explanation & diagrams — (5M)

Q10) a) Switching operation of transistor — (5M)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

IA-2 PERFORMANCE ANALYSIS

Internal Assessment 2

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
CO mapping	CO5	CO5	CO5	CO5	CO5	CO6	CO6	CO6	CO6	CO6
Max Marks /Question	10	10	10	10	10	10	10	10	10	10
Total marks of class /question	250	80	250	100	226	88	231	110	220	80
No. of students attended	25	8	25	10	23	9	24	11	23	8
No of students scored > 65% of marks/Question	25	8	25	10	23	9	23	11	23	8
Percentage of students scored>65% of marks/Question	100.00	100.00	100.00	100.00	100.00	100.00	95.84	100.00	100.00	100.00

Mark range	0-10	11 to 20	21 to 30	31-40	41-50
No. Of Students	0	0	0	0	33

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics and Communication Engineering

CONTINUOUS INTERNAL EVALUATION ASSESSMENT REPORT

Staff Name: Mr. Khaja Moinuddin/ Mrs Vani H **Sem/Sec:** 3/A&B **Academic year:** 20-21

Course Name: ED **Course code:** 18EC33 **CIE:** 2

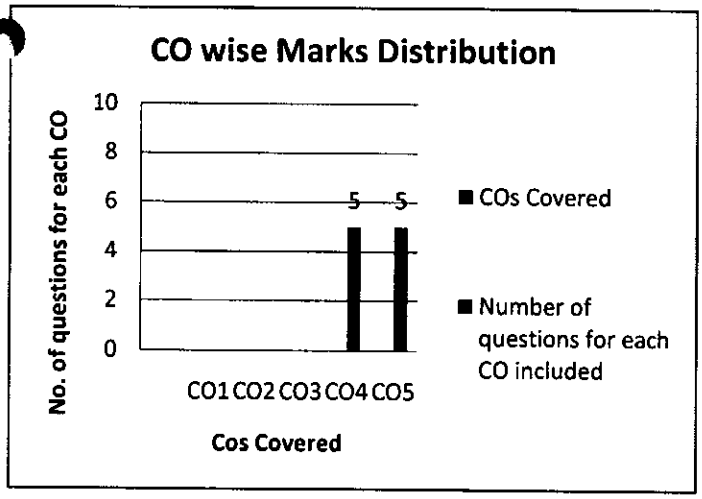
Mention the Syllabus included for CIE:

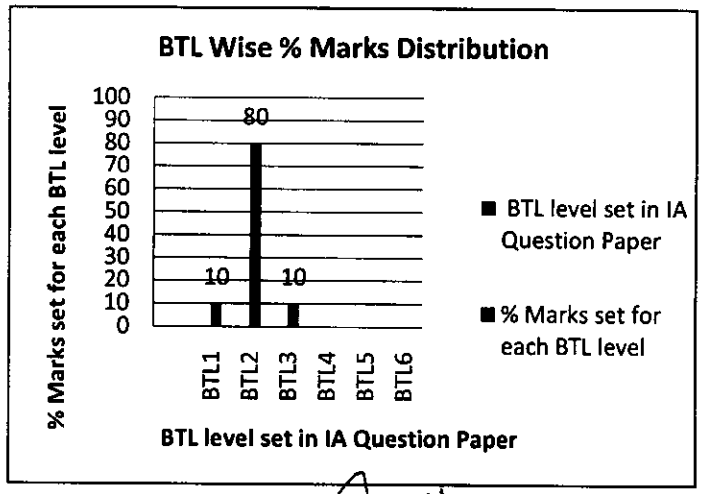
1	MODULE NUMBERS	3,4
2	CO s COVERED	CO4,CO5
3	BTL LEVELS ADDRESSED	L1,L2,L3

Mention following details of CIE Questions Paper setting :

1	COs Covered	CO1	CO2	CO3	CO4	CO5
					Y	Y
2	Number of questions for each CO				5	5

1	BTL level set in IA Question Paper	BTL1	BTL2	BTL3	BTL4	BTL5	BTL6
		Y	Y	Y			
2	% Marks set for each BTL level	10	80	10			





Staff Signature

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CONTINIOUS INTERNAL EVALUATION-III (20-21 Odd Sem)

Staff Name: Mr. Khaja Moinuddin / Mrs Vani H	**Sem: III** A /B	**Date: 13**/01/2021
Course Name: Electronic Devices	**Course Code:**18EC33	**Time :9.15-10.45AM**
Max marks: 50	**Prerequisites:** Basic Electronics	**Total Contact Hours :** 40

NOTE: Answer five questions (at least one from each pair of questions)

Q No	QUESTIONS	Marks	BTL	CO	PO	PSO
Q1	Describe low pressure chemical vapor deposition method	10	L2	3	1	
	OR					
Q2	Explain the process of Sio_2 deposition on Si wafer using Rapid Thermal processing with diagram	10	L2	3	1	
Q3	Discuss photolithography with necessary equations	10	L2	3	2	
	OR					
Q4	Explain the process of Sio_2 deposition on Si wafer using Thermal oxidation process with diagram and equations	10	L2	3	1	
Q5	Discuss Reactive Ion etching process with diagram	10	L2	3	1	
	OR					
Q6	Summarize the steps in fabrication of pn junction with diagrams	10	L2	3	1	
Q7	Discuss Solar cell with necessary diagrams	10	L2	2	1	
	OR					
Q8	Explain current and voltage in an illuminated junction with necessary equation and diagrams	10	L2	2	2	
Q9	a)Classify ICs based on application and fabrication b) List and Explain briefly advantages of Integration	4 6	L3 L1	3	1	
	OR					
Q10	Explain CMOS process Integration	10	L2	3	2	

IA Co-ordinator

Signature of faculty

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SCHEME OF EVALUATION-I (20-21 Odd Sem)

Staff Name: Mr. Khaja Moinuddin / Mrs Vani H	**Sem:** III A /B	**Date:** 18/10/2020
Course Name: Electronic Devices	**Course Code:**18EC33	**Time :9.15-10.45AM**
Max marks: 50	**Prerequisites:** Basic Electronics	**Total Contact Hours :** 40

Q1) Ionic bonding — 3M

Metallic bonding — 3M

Covalent bonding — 4M

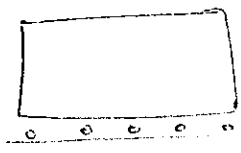
Q2) $\mu_n = \frac{-V_x}{\mathcal{E}_x}$ $\mu_p = \frac{V_x}{\mathcal{E}_x}$

$J_x = q n \mu_n \mathcal{E}_x$

$J_x = q(n\mu_n + p\mu_p)\mathcal{E}_x = \sigma \mathcal{E}_x$.

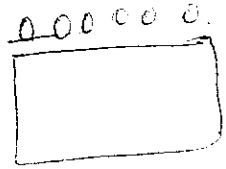
— 10M

Q3)



donar energy level

— 4M

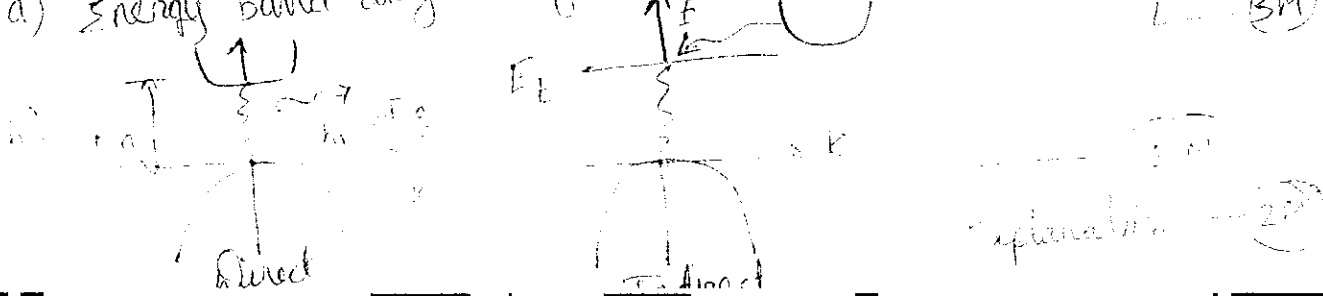


Acceptor energy level

N-type

Explanation — 6M

Q4) a) Energy band diagram for Insulators, Semiconductors, Metal — 3M

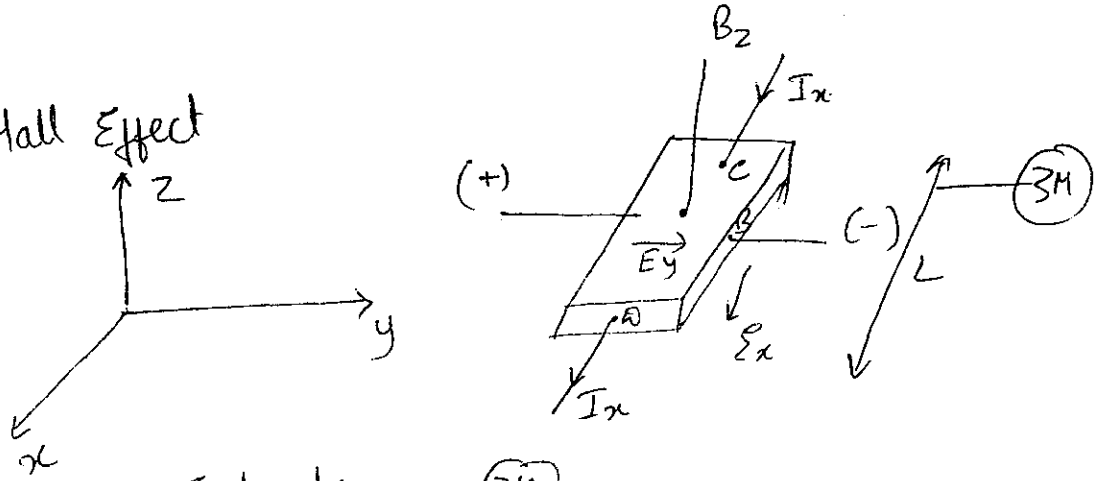


Explanation — 2M

Q5) a) Lattice Scattering — 5M

Impurity Scattering — 5M

Q6) Hall Effect



Explanation — 3M

Equation — 4M

Q7) Zener Breakdown

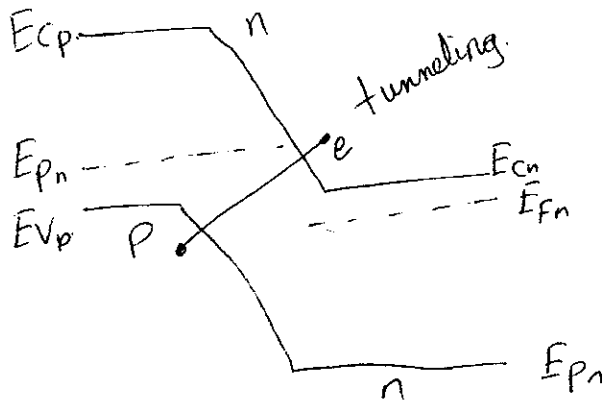
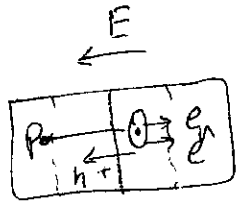


Diagram — 2M

Explanation — 3M



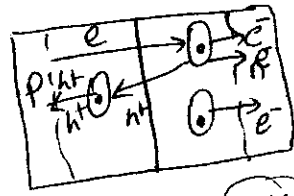


Diagram — 2M

Explanation — 3M

Q8) Forward Bias current flow with figures & explanation — 5M

Reverse Bias current flow with figures & explanation — 5M

Q9) Formation of Conduction band and Valence band

Explanation — 5M figures — 5M

Q10) a) Electron hole pair generation — 5M

b) [illegible] of charge carriers in semiconductor — 5M

Vani H

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

IA-3 PERFORMANCE ANALYSIS

Internal Assessment 3

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
CO mapping	CO3	CO3	CO3	CO3	CO3	CO3	CO2	CO2	CO3	CO3
Max Marks /Question	10	10	10	10	10	10	10	10	10	10
Total marks of class /question	218	70	100	176	232	76	76	129	79	146
No. of students attended	22	7	10	18	25	8	9	14	9	19
No of students scored > 65% of marks/Question	22	7	10	18	22	8	6	13	7	11
Percentage of students scored>65% of marks/Question	100.00	100.00	100.00	100.00	88.00	100.00	66.67	92.86	77.78	57.90

Mark range	0-10	11 to 20	21 to 30	31-40	41-50
No. Of Students	0	02	06	09	16

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics and Communication Engineering

CONTINUOUS INTERNAL EVALUATION ASSESSMENT REPORT

Staff Name: Mr. Khaja Moinuddin/ Mrs Vani H **Sem/Sec:** 3/A&B **Academic year:** 20-21

Course Name: ED **Course code:** 18EC33 **CIE:** 3

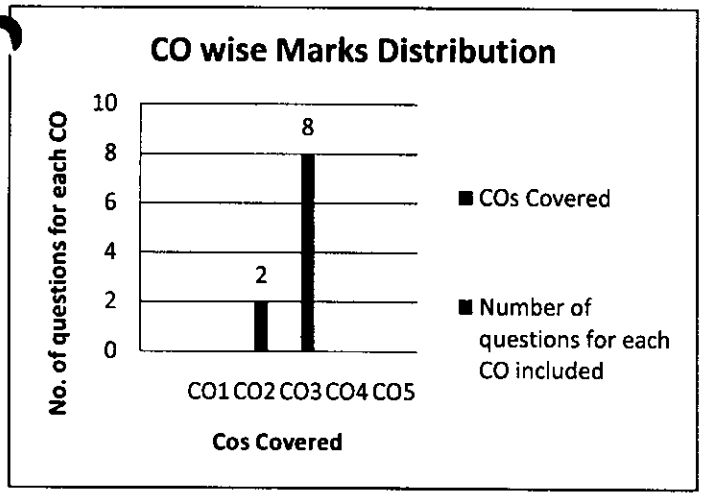
Mention the Syllabus included for CIE:

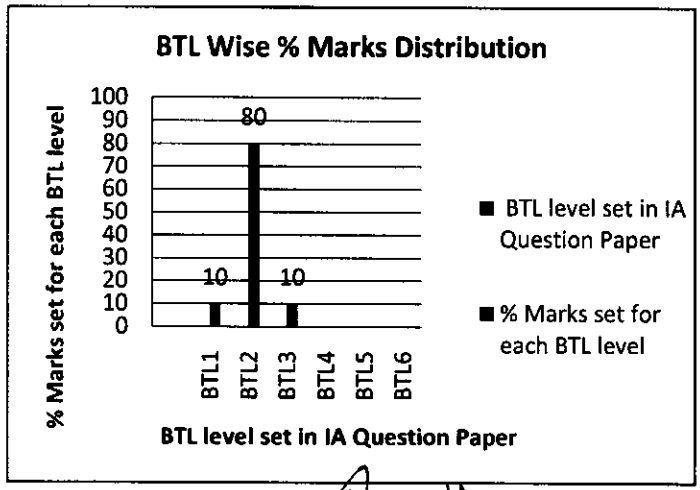
1	**MODULE NUMBERS**	5,2
2	**CO s COVERED**	CO2,CO3
3	**BTL LEVELS ADDRESSED**	L1,L2,L3

Mention following details of CIE Questions Paper setting :

1	**COs Covered**	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
			Y	Y		
2	**Number of questions for each CO**		2	8		

1	**BTL level set in IA Question Paper**	**BTL1**	**BTL2**	**BTL3**	**BTL4**	**BTL5**	**BTL6**
		Y	Y	Y			
2	**% Marks set for each BTL level**	10	80	10			





Staff Signature

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics and Communication Engineering

ASSIGNMENT-I (20-21 Odd Sem)

Staff Name : Khaja Moinuddin/ Vani H	**Sem/Sec:3rd /A & B**	**Max Marks:10**
Course Name : ED	**Course Code : 18EC33**	

Q No	QUESTIONS	CO	BTL
1	Explain different types of bonding forces in solids	1	2
2	Develop the equation for mobility of electron and holes ,current density in terms of conductivity	1	2
3	Explain extrinsic semiconductors with energy band diagram marking donor and acceptor energy level	1	2
4	Classify metals, semiconductors and insulator with energy band diagram	1	2
5	Explain direct and indirect semiconductors	1	2
6	Explain i)Lattice scattering ii) Impurity scattering	1	2
7	Explain Hall effectwith neat diagram and necessary equations	1	2
8	Explain a) Zener breakdown b) Avalanche breakdown	2	2
9	Explain formation of conduction and valence band when N atoms of silicon comes closer to form crystalline structure with diagram	1	2
10	Explain how electron hole pairs are created		2
11	discuss drift of charge carriers in semiconductor with diagram	1	2

Co-ordinator

Faculty Incharge

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics and Communication Engineering

ASSIGNMENT-II (20-21 Odd Sem)

Staff Name : Khaja Moinuddin/ Vani H	Sem/Sec:3rd /A & B	Max Marks:10
Course Name : ED	Course Code : 18EC33	

Q No	QUESTIONS	CO	BTL
1	Explain Operation of N-channel JFET with diagrams	5	2
2	Explain Operation of N-channel Enhancement MOSFET with diagrams	5	2
3	Explain ideal C-V characteristics with necessary equations and diagram	5	2
4	Discuss energy band diagram for p-channel MOS capacitor with positive and negative bias voltage	5	2
5	Explain small signal equivalent circuit with necessary equations	5	2
6	Explain pnp transistor in common base configuration mentioning requirement of good transistor	4	2
7	Explain how transistor works as an amplifier with all necessary factors equation and diagrams	4	2
8	Sketch the diagram showing hole and electron flow in pnp transistor and explain	4	3
9	Compute I_B and I_C assume τ_p=10μs τ_t=0.1μs R_B=50KΩ V_{BB}=5V	4	3
10	Discuss the concept of drift in base region with diagram and necessary equations		2
11	Explain switching operation for transistor in common emitter configuration	4	2
12	Define i)Rise time(tr) ii)Fall Time(tf)	4	1

Co-ordinator

Faculty Incharge

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

Department of Electronics and Communication Engineering

ASSIGNMENT-III (18-19 Odd Sem)

Staff Name : Khaja Moinuddin/ Vani H	Sem/Sec:3rd /A & B	Max Marks:10
Course Name : ED	Course Code : 18EC33	

Q No	QUESTIONS	CO	BTL
1	Describe low pressure chemical vapor deposition method	3	2
2	Explain the process of Sio_2 deposition on Si wafer using Rapid Thermal processing with diagram	3	2
3	Discuss photolithography with necessary equations	3	2
4	Explain the process of Sio_2 deposition on Si wafer using Thermal oxidation process with diagram and equations	3	2
5	Discuss Reactive Ion etching process with diagram	3	2
6	Summarize the steps in fabrication of pn junction with diagrams	3	2
7	Discuss Solar cell with necessary diagrams	2	2
8	Explain current and voltage in an illuminated junction with necessary equation and diagrams	2	2
9	Classify ICs based on application and fabrication	3	2
10	List and Explain briefly advantages of Integration		2
11	Explain CMOS process Integration	3	2

Co-ordinator

Faculty Incharge

V.V. Sangha's

Rao Bahadur Y Mahabaleswarappa Engineering College,Ballari

Dept. of Electronics & Communication Engineering

Assignment Evaluation Sheet - [1] for Odd Sem 2020-21

Sub/Code: ED/18EC33

Max Marks:10

Sem:3

Sec: A

Sl. No	USN	Student Name	Assignments / Unit tests/ Written Quizzes/ Associated Labs					
			Writing Skill (2 Marks)	Completeness (2 Marks)	Understanding (2 Marks)	Timely Submission (2 Marks)	Innovative Methods (2 Marks)	Total (10 Marks)
1	3VC19EC003	AMREEN TAJ M	2	2	2	2	2	10
2	3VC19EC004	AMRUTA G	2	2	2	2	2	10
3	3VC19EC005	ASLAM LANGOTI	2	2	2	2	2	10
4	3VC19EC006	B NAGABHARATH	2	2	2	2	2	10
5	3VC19EC007	BELLAM KONDA SIVA SAI	2	2	2	2	2	10
6	3VC19EC009	BHOOMIKA M U	2	2	2	2	2	10
7	3VC19EC017	J PUNITH	2	2	2	2	2	10
8	3VC19EC018	JOSHNA J A	2	2	2	2	2	10
9	3VC19EC021	K RAJASHEKAR REDDY	2	2	2	2	2	10
10	3VC19EC023	KAVITHA K	2	2	2	2	2	10
11	3VC19EC027	KURUVA SRINITHYA	2	2	2	2	2	10
12	3VC19EC028	M MEGHANA	2	2	2	2	2	10
13	3VC19EC029	M PALLAVI	2	2	2	2	2	10
14	3VC19EC030	M RAGHAVENDRA	2	2	2	2	2	10
15	3VC19EC031	M VYSHNAVI	2	2	2	2	2	10
16	3VC19EC032	MADHURI K V	2	2	2	2	2	10
17	3VC19EC034	MANOJ KUMAR K	2	2	2	2	2	10
18	3VC19EC037	N VENKATSAI	2	2	2	2	2	10
19	3VC19EC038	NIHARIKA M	2	2	2	2	2	10
20	3VC19EC040	P PRIYANKA	2	2	2	2	2	10

21	3VC19EC041	PALLAVI S	2	2	2	2	2	10
22	3VC19EC045	ROHIT BEJAWADA	2	2	2	2	2	10
23	3VC19EC047	SANDHYA S P	2	2	2	2	2	10
24	3VC19EC048	SARASWATHI S P	2	2	2	2	2	10
25	3VC19EC050	SHAIK MUSKAAN	2	2	2	2	2	10
26	3VC19EC052	SHIVANI B	2	2	2	2	2	10
27	3VC19EC055	SNEHA	2	2	2	2	2	10
28	3VC19EC058	SUDHAVANI A	2	2	2	2	2	10
29	3VC19EC060	UNNI KRISHANAN G	2	2	2	2	2	10
30	3VC19EC063	VAMSHI KRISHNA REDDY	2	2	2	2	2	10
31	3VC19EC066	VINOD KUMAR U	2	2	2	2	2	10
32	3VC17EC020	HARSHITHA R B	2	2	2	2	2	10

Staff Sign
VANI H

HOD ECE

V.V. Sangha's

Rao Bahadur Y Mahabaleswarappa Engineering College,Ballari

Dept. of Electronics & Communication Engineering

Assignment Evaluation Sheet - [2] for Odd Sem 2020-21

Sub/Code: ED/18EC33 **Max Marks:10**

Sem:3 Sec: A

Sl. No	USN	Student Name	Assignments / Unit tests/ Written Quizzes/ Associated Labs					
			Writing Skill (2 Marks)	Completeness (2 Marks)	Understanding (2 Marks)	Timely Submission (2 Marks)	Innovative Methods (2 Marks)	Total (10 Marks)
1	3VC19EC003	AMREEN TAJ M	2	2	2	2	2	10
2	3VC19EC004	AMRUTA G	2	2	2	2	2	10
3	3VC19EC005	ASLAM LANGOTI	2	2	2	2	2	10
4	3VC19EC006	B NAGABHARATH	2	2	2	2	2	10
5	3VC19EC007	BELLAM KONDA SIVA SAI	2	2	2	2	2	10
6	3VC19EC009	BHOOMIKA M U	2	2	2	2	2	10
7	3VC19EC017	J PUNITH	2	2	2	2	2	10
8	3VC19EC018	JOSHNA J A	2	2	2	2	2	10
9	3VC19EC021	K RAJASHEKAR REDDY	2	2	2	2	2	10
10	3VC19EC023	KAVITHA K	2	2	2	2	2	10
11	3VC19EC027	KURUVA SRINITHYA	2	2	2	2	2	10
12	3VC19EC028	M MEGHANA	2	2	2	2	2	10
13	3VC19EC029	M PALLAVI	2	2	2	2	2	10
14	3VC19EC030	M RAGHAVENDRA	2	2	2	2	2	10
15	3VC19EC031	M VYSHNAVI	2	2	2	2	2	10
16	3VC19EC032	MADHURI K V	2	2	2	2	2	10
17	3VC19EC034	MANOJ KUMAR K	2	2	2	2	2	10
18	3VC19EC037	N VENKATSAI	2	2	2	2	2	10
19	3VC19EC038	NIHARIKA M	2	2	2	2	2	10
20	3VC19EC040	P PRIYANKA	2	2	2	2	2	10

21	3VC19EC041	PALLAVI S	2	2	2	2	2	10
22	3VC19EC045	ROHIT BEJAWADA	2	2	2	2	2	10
23	3VC19EC047	SANDHYA S P	2	2	2	2	2	10
24	3VC19EC048	SARASWATHI S P	2	2	2	2	2	10
25	3VC19EC050	SHAIK MUSKAAN	2	2	2	2	2	10
26	3VC19EC052	SHIVANI B	2	2	2	2	2	10
27	3VC19EC055	SNEHA	2	2	2	2	2	10
28	3VC19EC058	SUDHAVANI A	2	2	2	2	2	10
29	3VC19EC060	UNNI KRISHANAN G	2	2	2	2	2	10
30	3VC19EC063	VAMSHI KRISHNA REDDY	2	2	2	2	2	10
31	3VC19EC066	VINOD KUMAR U	2	2	2	2	2	10
32	3VC17EC020	HARSHITHA R B	2	2	2	2	2	10

Staff Sign
VANI H

HOD ECE

V.V. Sangha's

Rao Bahadur Y Mahabaleswarappa Engineering College,Ballari

Dept. of Electronics & Communication Engineering

Assignment Evaluation Sheet - [3] for Odd Sem 2020-21

Sub/Code: ED/18EC33

Sem:3

Max Marks:10

Sec: A

Sl. No	USN	Student Name	Assignments / Unit tests/ Written Quizzes/ Associated Labs					
			Writing Skill (2 Marks)	Completeness (2 Marks)	Understanding (2 Marks)	Timely Submission (2 Marks)	Innovative Methods (2 Marks)	Total (10 Marks)
1	3VC19EC003	AMREEN TAJ M	2	2	2	2	2	10
2	3VC19EC004	AMRUTA G	2	2	2	2	2	10
3	3VC19EC005	ASLAM LANGOTI	2	2	2	2	2	10
4	3VC19EC006	B NAGABHARATH	2	2	2	2	2	10
5	3VC19EC007	BELLAM KONDA SIVA SAI	2	2	2	2	2	10
6	3VC19EC009	BHOOMIKA M U	2	2	2	2	2	10
7	3VC19EC017	J PUNITH	2	2	2	2	2	10
8	3VC19EC018	JOSHNA J A	2	2	2	2	2	10
9	3VC19EC021	K RAJASHEKAR REDDY	2	2	2	2	2	10
10	3VC19EC023	KAVITHA K	2	2	2	2	2	10
11	3VC19EC027	KURUVA SRINITHYA	2	2	2	2	2	10
12	3VC19EC028	M MEGHANA	2	2	2	2	2	10
13	3VC19EC029	M PALLAVI	2	2	2	2	2	10
14	3VC19EC030	M RAGHAVENDRA	2	2	2	2	2	10
15	3VC19EC031	M VYSHNAVI	2	2	2	2	2	10
16	3VC19EC032	MADHURI K V	2	2	2	2	2	10
17	3VC19EC034	MANOJ KUMAR K	2	2	2	2	2	10
18	3VC19EC037	N VENKATSAI	2	2	2	2	2	10
19	3VC19EC038	NIHARIKA M	2	2	2	2	2	10
20	3VC19EC040	P PRIYANKA	2	2	2	2	2	10

21	3VC19EC041	PALLAVI S	2	2	2	2	2	10
22	3VC19EC045	ROHIT BEJAWADA	2	2	2	2	2	10
23	3VC19EC047	SANDHYA S P	2	2	2	2	2	10
24	3VC19EC048	SARASWATHI S P	2	2	2	2	2	10
25	3VC19EC050	SHAIK MUSKAAN	2	2	2	2	2	10
26	3VC19EC052	SHIVANI B	2	2	2	2	2	10
27	3VC19EC055	SNEHA	2	2	2	2	2	10
28	3VC19EC058	SUDHAVANI A	2	2	2	2	2	10
29	3VC19EC060	UNNI KRISHANAN G	2	2	2	2	2	10
30	3VC19EC063	VAMSHI KRISHNA REDDY	2	2	2	2	2	10
31	3VC19EC066	VINOD KUMAR U	2	2	2	2	2	10
32	3VC17EC020	HARSHITHA R B	2	2	2	2	2	10

Staff Sign

VANI H

HOD ECE

Rao Bahadur Y Mahabaleswarappa Engineering College
Dept. of Electronics & Communication Engineering
Semester :3RD A

3/A ED

Sl. No	USN NO	NAME	CIE	Assgn	SEE
1	3VC19EC003	AMREEN TAJ M	35	10	11
2	3VC19EC004	AMRUTA G	38	10	17
3	3VC19EC005	ASLAM LANGOTI	39	10	21
4	3VC19EC006	B NAGABHARATH	38	10	40
5	3VC19EC007	BELLAM KONDA SIVA SAI	37	10	8
6	3VC19EC009	BHOOMIKA M U	39	10	33
7	3VC19EC017	J PUNITH	38	10	27
8	3VC19EC018	JOSHNA J A	36	10	21
9	3VC19EC019	K B CHANDRASHEKAR	40	10	32
10	3VC19EC021	K RAJASHEKAR REDDY	40	10	35
11	3VC19EC023	KAVITHA K	33	10	8
12	3VC19EC027	KURUVA SRINITHYA	37	10	35
13	3VC19EC028	M MEGHANA	38	10	29
14	3VC19EC029	M PALLAVI	39	10	12
15	3VC19EC030	M RAGHAVENDRA	38	10	27
16	3VC19EC031	M VYSHNAVI	40	10	24
17	3VC19EC032	MADHURI K V	33	10	33
18	3VC19EC034	MANOJ KUMAR K	40	10	42
19	3VC19EC037	N VENKATSAI	39	10	37
20	3VC19EC038	NIHARIKA M	40	10	21
21	3VC19EC040	P PRIYANKA	38	10	21
22	3VC19EC041	PALLAVI S	30	10	21
23	3VC19EC045	ROHIT BEJAWADA	36	10	17
24	3VC19EC047	SANDHYA S P	31	10	9
25	3VC19EC048	SARASWATHI S P	36	10	29
26	3VC19EC050	SHAIK MUSKAAN	35	10	10
27	3VC19EC052	SHIVANI B	39	10	21
28	3VC19EC055	SNEHA	39	10	32
29	3VC19EC058	SUDHAVANI A	39	10	21
30	3VC19EC060	UNNI KRISHANAN G	33	10	12
31	3VC19EC063	VAMSHI KRISHNA REDDY C	39	10	30
32	3VC19EC066	VINOD KUMAR U	40	10	40
33	3VC17EC020	HARSHITHA R B	34	10	21

Rao Bahadur Y Mahaleswarappa Engineering College

Dept. of Electronics & Communication Engineering

Semester :3RD A **AY 2020-21**

Course exit survey for ED

At the end of the course, students will be able to ....

C203.1	Understand the principles of semiconductor physics
C203.2	Understand the principles and characteristics of different types of semiconductor devices
C203.3	Understand the fabrication process of semiconductor devices and integrated circuits
C203.4	Discuss the operation of BJT, Ebers moll coupled diode model ,cutoff , saturation and switching operation of transistor
C203.5	Understand the mathematical models of semiconductor junction and MOS transistors for circuits and systems

Course Exit Survey Guidelines: Excellent – 5, Very Good – 4, Good – 3,Average – 2, Below Average - 1

3VC19EC002	ABHISHEK A M	5	3	3	4	1	
3VC19EC003	AMREEN TAJ M	4	3	3	4	4	
3VC19EC005	ASLAM LANGOTI	3	3	4	3	4	
3VC19EC006	B NAGABHARATH	3	3	4	3	4	
3VC19EC007	BELLAM KONDA SIVA SAI	4	4	3	3	4	
3VC19EC009	BHOOMIKA M U	3	3	3	2	3	Bhoomika M.U
3VC19EC013	GANGADHARA A	4	3	4	3	4	
3VC19EC015	H MEGHANA	5	3	3	4	4	
3VC19EC017	J PUNITH	3	3	3	3	4	J.Punith
3VC19EC018	JOSHNA J A	4	4	4	3	4	Joshna JA
3VC19EC019	K B CHANDRASHEKAR	3	4	3	4	3	
3VC19EC021	K RAJASHEKAR REDDY	3	3	3	2	3	
3VC19EC023	KAVITHA K	3	3	3	3	3	K.Kavitha
3VC19EC029	M PALLAVI	4	3	3	3	3	
3VC19EC030	M RAGHAVENDRA	4	3	4	3	3	
3VC19EC032	MADHURI K V	4	4	3	3	3	
3VC19EC034	MANOJ KUMAR K	3	4	3	3	3	
3VC19EC036	MOHMMEDJUNAID A NAMAJKATTI	4	4	4	3	3	
3VC19EC037	N VENKATSAI	5	3	5	3	3	Venkat Sai
3VC19EC038	NIHARIKA M	4	3	5	3	4	
3VC19EC040	P PRIYANKA	4	4	3	4	3	
3VC19EC041	PALLAVI S	5	4	3	4	5	
3VC19EC045	ROHIT BEJAWADA	3	3	3	3	3	

3VC19EC045	ROHIT BEJAWADA	4	4	3	4	4	
3VC19EC047	SANDHYA S P	4	4	4	4	4	Sandhya
3VC19EC048	SARASWATHI S P	4	4	3	3	4	
3VC19EC050	SHAIK MUSKAAN	4	4	4	4	4	
3VC19EC052	SHIVANI B	4	3	4	3	4	
3VC19EC055	SNEHA	5	4	5	4	5	
3VC19EC058	SUDHAVANI A	5	4	5	4	3	
3VC19EC060	UNNI KRISHANAN G	3	4	3	2	3	Krishnan
3VC19EC062	VAMSHI KRISHNA K	4	3	4	3	4	
3VC19EC063	VAMSHI KRISHNA REDDY C	5	4	5	3	5	Vamshi
3VC19EC066	VINOD KUMAR U	5	5	5	5	5	U. Vinod Kumar
3VC17Ec020	HARSHITHA R B	3	4	3	4	3	
3VC19EC027	K. SRIVATHYA	4	3	4	3	3	
3VC19EC031	M. Vyshnavi	5	4	5	4	5	
3VC19EC004	Amruta.G.	4	3	3	4	3	Amruta.G.
3VC19EC028	M. Meghana	4	3	4	3	3	M. Meghana

Rao Bahadur Y Mahabaleswarappa Engineering College

Dept. of Electronics & Communication Engineering

Semester :3RD A **AY 2020-21**

Questionnaires for ED

Q1	Are you able to classify materials based on energy band diagram
Q2	Are you able to understand drift of charge carriers in semiconductor
Q3	Are you able to understand biasing of pn junction
Q4	Are you able to understand concept of photo detector
Q5	Are you able to explain how transistor works as an amplifier
Q6	Are you able to explain base narrowing
Q7	Are you able to explain operation of JFET
Q8	Are you able to differentiate between depletion and enhancement MOSFET
Q9	Are you able to List the steps for fabrication of PN junction
Q10	Are you able to understand CMOS structure

Questionnairies Guidelines: Excellent – 5, Very Good – 4, Good – 3,Average – 2, Below Average - 1

		Question										
3VC19EC003	AMREEN TAJ M	4	4	3	3	4	4	3	3	4	4	
3VC19EC004	AMRUTA G	4	4	3	3	4	3	4	3	3	3	Amruta.G.
3VC19EC005	ASLAM LANGOTI	3	4	3	3	4	5	4	3	3	5	
3VC19EC006	B NAGABHARATH	3	4	3	3	4	4	3	3	4	3	
3VC19EC007	BELLAM KONDA SIVA SAI	4	4	4	3	3	4	4	3	4	3	
3VC19EC009	BHOOMIKA M U	3	4	3	3	3	3	3	2	3	3	
3VC19EC013	GANGADHARA A	4	3	4	3	4	3	3	4	4	4	
3VC19EC017	J PUNITH	3	3	4	4	3	4	4	3	4	3	J.Punith
3VC19EC018	JOSHNA J A	4	3	3	4	4	3	4	3	3	4	
3VC19EC019	K B CHANDRASHEKAR	3	4	3	3	3	4	3	3	3	4	
3VC19EC021	K RAJASHEKAR REDDY	3	4	3	3	3	3	3	2	3	3	
3VC19EC023	KAVITHA K	3	4	3	4	3	3	4	4	4	4	K.Kavitha
3VC19EC027	KURUVA SRINITHYA	3	4	5	4	4	3	2	5	4	4	

3VC19EC028	M MEGHANA	4	3	5	3	4	3	4	3	3	4	M
3VC19EC029	M PALLAVI	4	3	4	3	4	3	4	3	3	4	
3VC19EC030	M RAGHAVENDRA	4	4	3	3	4	4	3	3	4	3	
3VC19EC031	M VYSHNAVI	4	3	2	3	4	2	4	2	3	3	
3VC19EC032	MADHURI K V	4	3	4	3	4	3	4	4	3	3	
3VC19EC034	MANOJ KUMAR K	4	4	4	3	3	3	4	4	3	3	
3VC19EC037	N VENKATSAI	4	3	4	5	3	2	4	3	3	4	
3VC19EC038	NIHARIKA M	3	4	5	4	4	3	2	5	4	4	
3VC19EC040	P PRIYANKA	4	3	4	3	3	3	4	4	3	4	
3VC19EC041	PALLAVI S	4	3	4	4	3	4	4	3	3	4	
3VC19EC045	ROHIT BEJAWADA	3	2	3	2	3	4	4	4	4	4	
3VC19EC047	SANDHYA S P	4	4	4	4	4	4	4	4	4	4	
3VC19EC048	SARASWATHI S P	4	4	3	3	4	4	3	3	4	4	
3VC19EC050	SHAIK MUSKAAN	3	3	3	4	3	3	3	4	3	3	
3VC19EC052	SHIVANI B	4	4	3	3	4	4	3	3	4	4	
3VC19EC055	SNEHA	4	3	2	3	4	2	4	4	2	3	
3VC19EC058	SUDHAVANI A	4	3	2	3	4	2	4	4	2	3	A. Sudha
3VC19EC060	UNNI KRISHANAN G	2	3	4	4	3	2	4	4	4	3	
3VC19EC062	VAMSHI KRISHNA K	3	4	3	4	3	4	3	4	3	4	
3VC19EC063	VAMSHI KRISHNA REDDY C	4	3	4	4	3	2	3	3	4	3	
3VC19EC066	VINOD KUMAR U	5	5	5	5	5	5	5	5	5	5	
3VC17Ec020	HARSHITHA R B	4	4	5	3	3	4	4	3	3	3	

Faculty: VANI H					
Course Name: ELECTRONIC DEVICES					
Course Code: 18EC33					
Academic Year: 2020-21					
Sl. No	USN NO	NAME	CIE	SEE	Total
1	3VC19EC003	AMREEN TAJ M	35		46
2	3VC19EC004	AMRUTA G	38		55
3	3VC19EC005	ASLAM LANGOTI	39	21	60
4	3VC19EC006	B NAGABHARATH	38	40	78
5	3VC19EC007	BELLAM KONDA SIVA SAI	37		45
6	3VC19EC009	BHOOMIKA M U	39	33	72
7	3VC19EC017	J PUNITH	38	27	65
8	3VC19EC018	JOSHNA J A	36	21	57
9	3VC19EC019	K B CHANDRASHEKAR	40	32	72
10	3VC19EC021	K RAJASHEKAR REDDY	40	35	75
11	3VC19EC023	KAVITHA K	33		41
12	3VC19EC027	KURUVA SRINITHYA	37	35	72
13	3VC19EC028	M MEGHANA	38	29	67
14	3VC19EC029	M PALLAVI	39		51
15	3VC19EC030	M RAGHAVENDRA	38	27	65
16	3VC19EC031	M VYSHNAVI	40	24	64
17	3VC19EC032	MADHURI K V	33	33	66
18	3VC19EC034	MANOJ KUMAR K	40	42	82
19	3VC19EC037	N VENKATSAI	39	37	76
20	3VC19EC038	NIHARIKA M	40	21	61
21	3VC19EC040	P PRIYANKA	38	21	59
22	3VC19EC041	PALLAVI S	30	21	51
23	3VC19EC045	ROHIT BEJAWADA	36		53
24	3VC19EC047	SANDHYA S P	31		40
25	3VC19EC048	SARASWATHI S P	36	29	65
26	3VC19EC050	SHAIK MUSKAAN	35		45
27	3VC19EC052	SHIVANI B	39	21	60
28	3VC19EC055	SNEHA	39	32	71
29	3VC19EC058	SUDHAVANI A	39	21	60
30	3VC19EC060	UNNI KRISHANAN G	33		45

31	3VC19EC063	VAMSHI KRISHNA REDDY C	39	30	69
32	3VC19EC066	VINOD KUMAR U	40	40	80
33	3VC17EC020	HARSHITHA R B	34	21	55
34					
35					
36					
37					
38					
Number of students scoring >= 27 in EXTERNAL				**15**	

EXTERNAL EXAM

Number of students appeared for the exam	**33**		-
Number of students scoring >= 45% in EXTERNAL	**15**		-
Percentage	**0.45**		-
Achieved target:	**45%**		
ATTAINMENT LEVEL	1		

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARIDEPARTMENT OF ELECTRONICS COMMUNICATION ENGNEERING

DIRECT & INDIRECT ATTAINMENT 2020-21

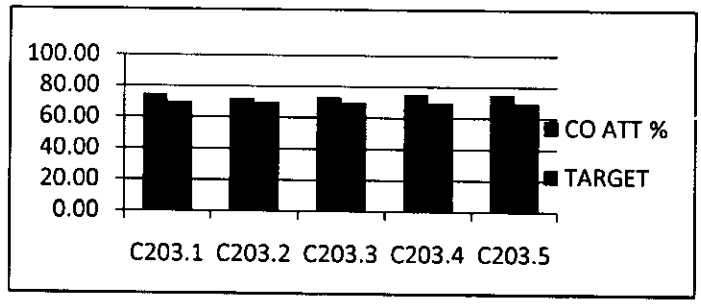
Faculty: VANI H					
Course Name: ELECTRONIC DEVICES					
Course Code:18EC33	**Sem**	**3**	**Sec**	**A**	

C203.1	Understand the principles of semiconductor physics
C203.2	Understand the principles and characteristics of different types of semiconductor devices
C203.3	Understand the fabrication process of semiconductor devices
C203.4	Discuss the operation of BJT, Ebers moll coupled diode model ,cutoff , saturation and switching
C203.5	Understand the mathematical models of semiconductor junction and MOS transistors for circuits and

CO-PO/PSO Mapping

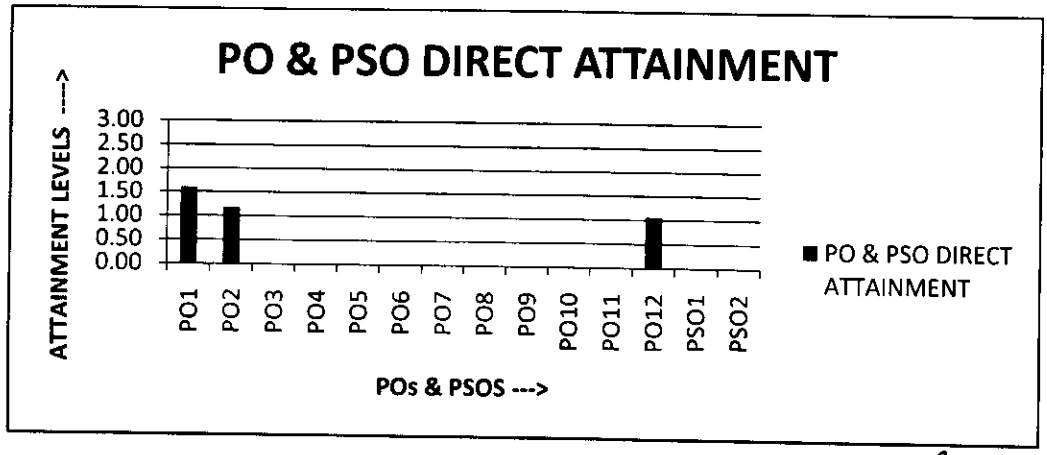
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
C203.1	3	2										2		
C203.2	3	2										2		
C203.3	3											2		
C203.4	3	2										2		
C203.5	3	2										2		
AVG	3.00	2.00										2.00		

	CO AT	TARGET
C203.1	74.73	70
C203.2	72.26	70
C203.3	73.12	70
C203.4	75.42	70
C203.5	75.42	70



	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
PO ATT	1.60	1.17										1.07		

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
PO ATT	3.00	2.00										2.00		



Vani H

CO ATTAINMENT GAP ANALYSIS 2020-21 (ODD)ED

Course Outcomes	CO Attainment	CO Target	CO Attainment Gap	CO Attainment Level
C203.1	74.73	70	NO GAP	3
C203.2	72.26	70	NO GAP	3
C203.3	73.12	70	NO GAP	3
C203.4	75.42	70	NO GAP	3
C203.5	75.42	70	NO GAP	3

ACTION REPORT ON GAP ANALYSIS

Course Outcomes	Action proposed to bridge the gap	Modification of target if achieved
C203.1		75
C203.2		75
C203.3		75
C203.4		75
C203.5		75

INSTRUCTOR REPORT: 2020-21

Impact of Delivery Methods (state the delivery methods used and its effectiveness):

- **Blended method**: This subject was taught in blended mode both in offline and online mode due to pandemic again for the second time; offline teaching method was effective compared to online teaching. In online teaching shared presentations, done live classes and digital notes on high priority in Google classrooms, Gmeet and Zoom platforms.
- **Teaching-Learning**: After teaching each module students are assigned with video assignments and positively students made video lessons which is outcome based knowledge i.e student rather than just remembering the concepts and reproducing in exams now student started thinking and applying, the knowledge analyzing and presenting skills are improved.

Course Outcome Attainment Remarks: All Course outcomes are attained even after increasing attainment level from 65 to 70.

Instructor Feedback: Overall the subject Electronic Devices is theoritical. Hence student's centric approach is adapted to exhibit teaching methodologies.

Scope for improvement: Overall this subject attainment increases if we use outcome based student centric approach which reflects in securing good score as well gaining knowledge which is directly proportional to improvements in attainment levels.

CBCS SCHEME

USN | | | | | | | | | | |

18EC33

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. What are the types of Bonding forceses in solids? Explain. **(06 Marks)**

b. Explain the classification of material based on conductivity and energy band diagram. **(08 Marks)**

c. Find the conductivity of the intrinsic germanium at 300 K. If a donar type impurity is added to the extent of 1 atom/10^7 germanium atom assume $\mu_n = 3800$, $\mu_p = 1800$, $n_i = 2.5 \times 10^3$, $Q = 1.602 \times 10^{-19}$. **(06 Marks)**

OR

2 a. What are Direct and Indirect band gap semiconductor? Explain with examples. **(08 Marks)**

b. Explain the concentration of electron-hole pair in Intrinsic semiconductor with energy band diagram. **(06 Marks)**

c. Calculate the Intrinsic carrier concentration in Silicon at room temperature T = 300 K, where B is the material dependent parameter 5.4×10^{31} and E_g as the band gap energy 1.12 eV, where K is the Boltzmann constant 8.62×10^{-5} eV/K. **(06 Marks)**

Module-2

3 a. With energy band diagram, explain the doping level in extrinsic semiconductor at 0 K and at 50 K. **(09 Marks)**

b. What is the magnitude of HALL voltage in a N-Type germanium bar having an majority carrier concentration $N_D = 10^{17}$ cm^3. Assume B = 0.2 Wb/m^2, d = 2 mm, E = 10 V/cm. **(05 Marks)**

c. Explain the effect of temperature on semiconductor. **(06 Marks)**

OR

4 a. Explain the qualitative description of current flow at P-N junction under equilibrium and biased condition. **(08 Marks)**

b. Explain zener breakdown and avalanche breakdown under reverse biased P-N junction. **(06 Marks)**

c. Discuss the piece-wise linear approximations of junction diode under ideal condition. **(06 Marks)**

Module-3

5 a. Explain the optical generation of carrier in a P-N junction. **(08 Marks)**

b. Discuss the configuration of a solar cell in enlarged view of the planar junction. **(06 Marks)**

c. What is injection-electroluminiscence and what are its applications? **(06 Marks)**

OR

6 a. Explain I-V characteristics of n-p junction as a function of emitter current. **(08 Marks)**

b. Discuss switching operation in common-emitter transistor. **(06 Marks)**

c. Figure Q6 (c) shows the common emitter amplifier circuit. Calculate I_B and I_C assume $\tau_p = 10\,\mu s$, $\tau_i = 0.1\,\mu s$ **(06 Marks)**

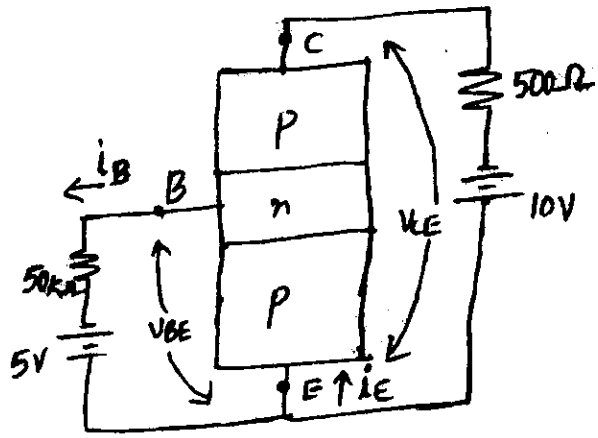


Fig. Q6 (c)

Module-4

7 a. Draw and explain the I-V characteristics of n-channel PNJFET for different biasing voltages. **(07 Marks)**

b. Draw and explain the small signal equivalent circuit of n-channel PNJFET. **(07 Marks)**

c. Explain the MOS structure with the aid of parallel-plate capacitor. **(06 Marks)**

OR

8 a. Explain the effect of frequency on gate voltage of a MOS capacitor with a P-type substrate. **(10 Marks)**

b. Explain P-channel enhancement and depletion type MOSFET with their circuit symbols. **(10 Marks)**

Module-5

9 a. With schematic diagram, explain ION-implantation system. **(07 Marks)**

b. Explain low pressure chemical vapour deposition reactor. **(07 Marks)**

c. Discuss photolithography. **(06 Marks)**

OR

10 a. What are the different types of integrated circuits and its advantages? **(10 Marks)**

b. Explain the process of Integration. **(10 Marks)**

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