VISION AND MISSION OF THE INSTITUTE AND DEPARTMENT

VISION OF THE INSTITUTION

To Produce Professionally Excellent, Knowledgeable, Globally Competitive and Socially Responsible Engineers and Entrepreneurs.

MISSION OF THE INSTITUTION

M1	To Provide Quality Education in Engineering and Management.
M2	To Establish a Continuous Industry-Institute Interaction, Participation and Collaboration to Contribute Skilled Engineers.
M3	To Develop Human Values, Social Values, Entrepreneurship Skills and Professional Ethics among the Technocrats.
M4	To Focus on Innovation and Development of Technologies by Engaging in Cutting Edge Research areas.

VISION OF THE DEPARTMENT

To Produce Professionally Excellent, Knowledgeable, Globally Competitive and Socially Responsible Electronics and Communication Engineers and Entrepreneurs.

MISSION OF THE DEPARTMENT

M1	To Provide Quality Education in Electronics and Communication Engineering.
M2	To Establish a Continuous Industry-Institute Interaction, Participation and Collaboration to Contribute Skilled Electronics and Communication Engineers.
M3	To Develop Human Values, Social Values, Entrepreneurship Skills and Professional Ethics among the Technocrats.
M4	To Focus on Innovation and Development of Technologies by Engaging in Electronics and Communication Research areas.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1	Graduates of Electronics & Communication Engineering course will have successful professional career.
PEO2	Graduates of Electronics & Communication Engineering course will pursue higher education or to become an Entrepreneur.
PEO3	Graduates of Electronics & Communication Engineering course will have ability for lifelong learning and to serve the society.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO 1	Ability to Design, Develop and Test the Electronics Circuits & Communication Systems.
PSO 2	Ability to Develop Excellent Programming and Problem Solving skills in the field of Embedded System.

PROGRAM OUTCOMES (PO)

PO 1	**Engineering Knowledge**	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem Analysis**	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design/ Development of Solutions**	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems**	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage**	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and society**	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability**	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	**Individual and team work**	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication**	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance**	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning**	Recognize the need for, and have the preparation and ability to engage in Independent and life-long learning in the broadest context of technological change.

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

Name of the Staff: Mr. PHANINDRA REDDY, Mr. CHANNAVEERANA GOUDA				
Course Name: REAL TIME SYSTEM				
Course Code: 17EC743	Sem:	7	Year	2020-21

COURSE OUTCOME STATEMENTS	
	At the end of the course, students will be able to ....
C404.1	Explain the fundamentals of real time systems, its classificationand Understand the concepts of computer control
C404.2	Describe computer hardware requirement for real time applications
C404.3	Summarize programming language basics for real time application
C404.4	Describe the operating system concepts and techniques required for real time system
C404.5	Explain various methodologies used for designing a real time system

CO-PO/PSO Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
C404.1	3													
C404.2	3	2												
C404.3	3	2												
C404.4	3	2												
C404.5	2		2											
AVG	2.8	2.00	2.00											

CO	PO	Mapping	Justification
C404.1	PO1	3	The student uses the basic knowledge of Engineering fundamentals to understand the basics of Real Time Systems and application of computers in Real Time Systems
C404.2	PO1	3	The student uses the basic knowledge of engineering fundamentals to understand components of computers and hardware used in real time system
	PO2	2	The student uses the knowledge of engineering to handle interrupts
C404.3	PO1	3	The student uses the knowledge of engineering fundamentals to understand concepts of Real Time Operating System
	PO2	2	The student uses the knowledge of engineering to provide solution to problem of mutual exclusion
C404.4	PO1	3	The student uses the engineering knowledge to understand phases of development of RTS.
	PO2	2	Students will be able to solve problems of real time design
C404.5	PO1	2	Students will be able to understand different methodologies
	PO3	2	Students will be able to design and develop real time system using different methodologies

Course Coordinator

Staff Signature

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

CO Analysis

Name of the Staff: Mr. PHANINDRA REDDY, Mr. CHANNAVEERANA GOUDA				
Course Name: REAL TIME SYSTEM				
Course Code: 17EC743	Sem:	7	Year	2020-21

CO	Description
C404.1	Explain the fundamentals of real time systems, its classificationand Understand the concepts of computer control **Action:** Explain **Knowledge:** • Fundamentals of real time systems • Its classification • Understand the concepts of computer control **Condition:** None **Criterion:** None
C404.2	Describe computer hardware requirement for real time applications **Action:** Describe **Knowledge:** • Computer hardware requirement **Condition**: For real time applications **Criterion:** None
C404.3	Summarize programming language basics for real time application **Action:** • Summarize **Knowledge:**Programming language basics **Condition:**For real time application **Criterion:** None
C404.4	Describe the operating system concepts and techniques required for real time system **Action:** • Describe **Knowledge:** Operating system concepts and techniques required **Condition:**For real time system **Criterion:**None
C404.5	Explain various methodologies used for designing a real time system **Action:** • Explain **Knowledge:**Various Methodologies **Condition:** Used for designing a real time system **Criterion:**None

Staff Signature

Tentative Academic Calendar of VTU, Belagavi for ODD Semester of 2020-2021

	I Sem B. E. / B. Tech. / B. Arch./B.Plan	I sem M.Tech./MBA /MCA/M.Arch.	III, V & VII Sem B. E. /B. Tech./B.Plan/ B.Arch & IX Sem B. Arch.	III & V Sem MCA	III Sem MBA	III Sem M. Tech.	III Sem M. Arch.
Commencement of ODD Semester	Will be announced later	Will be announced later	01.09.2020	01.09.2020	01.09.2020	01.09.2020	01.09.2020
Last Working day of ODD Semester			17.12.2020	17.12.2020	17.12.2020	17.12.2020	17.12.2020
Practical Examinations			21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020	21.12.2020 To 31.12.2020
Theory Examinations			04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021	04.01.2021 To 23.01.2021
Internship Viva-Voce			-	-	-	**25.01.2021 To 08.02.2021**	-
Professional training / Organization study			-	-	-		-
Commencement of EVEN Semester			08.02.2021	08.02.2021	08.02.2021	22.02.2021	08.02.2021

NOTE

- VII Semester B. E / B. Tech students shall have to undergo INTERNSHIP as per circular of University **VTU/Aca/2019-20/85, dated 12.05.2020.**
- I Semester B. E/ B. Tech / B. Arch Students shall compulsorily undergo Induction Program for a period of 3 Weeks as per the schedule given by VTU Belagavi
- The classroom sessions for all the higher semesters would be commencing from 01.09.2020(Tentative) in ONLINE mode until further orders.
- The Institute needs to function for six days a week with additional hours.
- The faculty/staff shall be available to undertake any work assigned by the university.
- If any of the above date is declared to be a holiday then the corresponding event will come into effect on the next working day.
- Notification regarding Calendar of Events relating to the conduct of University Examinations will be issued by the Registrar (Evaluation) from time to time.
- **Academic Calendar may be modified based on guidelines/directions issued in future by MHRD/UGC/AICTE/State Government.**

13.9.2020.

REGISTRAR

V.V. Sangha's
ರಾವ್ ಬಹದ್ದೂರ್ ವೈ. ಮಹಾಬಲೇಶ್ವರಪ್ಪ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜ್, ಬಳ್ಳಾರಿ
Rao Bahadur Y. Mahabaleswarappa Engineering College, Ballari
Cantonment, Ballari-583104. Tel: 08392-244809. Fax: 08392-242148

ACADEMIC CALENDAR 2020-21 (ODD SEM)

MONTH	DAY	DATE	EVENT	DESCRIPTION
September	Tuesday	01-09-2020	Commencement of ODD Semester	UG:-III,V,VII Sem Commencement of Classes.
	Tuesday	01-09-2020		PG:- III Sem Commencement of Classes.
	Monday	07-09-2020	Submission of Workload	Submit Final Faculty Teaching Workload.
	Saturday	19-09-2020	Parents Meet	Parents Meet should be arranged only for 3rd & 5th Sem Students
	Monday	21-09-2020	Course File Verification	Verification of Course plan & CO,PO Mapping
October	[illegible]	[illegible]	[illegible]	[illegible]
	Saturday	24/10/2020	Submit I-IA Marks	Enter I-IA Marks in RYMEC Online Portal on or Before said Date.
	Tuesday	27/10/2020	IA Reports to Parents	Dispatch of I-IA Marks , Attendance % through SMS to Parents on or Before said Date.
	Wednesday	28/10/2019	First Assignment Submission	Student should submit 1st Assignment on or before said date.
	Thursday	29/10/2020	Interaction with Parents	Interaction with Parents & Students Performance Review
November	Monday	02-11-2020	Verifying the Course file	Verifying the Assessment Strategies
	[illegible]	[illegible]	[illegible]	[illegible]
	Wednesday	25-11-2020	Submit II-IA Marks	Enter II-IA Marks in RYMEC Online Portal Before said Date.
	Saturday	26-11-2020	IA Reports to Parents	Dispatch of II-IA Marks , Attendance % through SMS to Parents on or Before said Date.
	Monday	27-11-2020	First Assignment Submission	Student should submit 2nd Assignment on or before said date.
	Saturday	05-12-2020	Interaction with Parents	Interaction with Parents & Students Performance Review
	Monday	07-12-2020	Verifying the Course file	Verifying the Assessment Strategies
December	[illegible]	[illegible]	[illegible]	[illegible]
	Wednesday	18/12/2020	Submit III-IA Marks	Enter III-IA Marks in RYMEC Online Portal Before said Date.
	Thursday	19/12/2020	IA Reports to Parents	Dispatch of III-IA Marks, Attendance % & Final Average Marks through SMS to Parents on or Before said Date.
	Thursday	17-12-2020	Last Working Day of Odd Sem 2020-21	UG:-III,V,VII Sem Last Working Day
	Thursday	17-12-2020		PG:-III Sem Last Working Day

RaoBahadur Y Mahabaleswarappa Engineering College, Ballari
Department of Electronics and Communication Engineering

Academic Calendar of Events
ODD Semester 2020-21(SEP 2020-March 2021)

	III, V& VII Sem B.E/B.Tech	III Sem M.Tech
Pre Placement Training	For VI Semester Students of all Branches from 20th to 25th Sep2020	
Commencement of ODD Semester	1st SEP 2020	
Admission Publicity in and around Ballari	SEP & OCT 2020	
I Internal Assessment Test	17th, 18th & 19th OCT 2020 (Sat, Sun & Mon-Online)	
One day Online FDP on **"Virtual Lab"** organized by VTU in collaboration with NITKSuratkal by Dr. K.V. Gangadharan	21st OCT 2020	
Last date for sending IA Marks (SMS)	27th OCT 2020	
Parents Meet	29th OCT 20220	
II Internal Assessment Test	1st, 2nd & 3rd DEC 2020 (Tue, Wed & Thu-Online)	
Last date for sending IA Marks (SMS)	6th DEC 2020	
Parents Meet	9th DEC 2020	
Fresher's Day & First Year Student Induction Programme through Digital Platform	17th DEC 2020	
Student Induction Programme **UHV Session-2** through Digital Platform for 1st Year Students	19th DEC 2020	
One day Seminar On **"FUTURE READY: Industry 4.0"** by Mr. MKHH Jilani, Investment banker & Strategic advisor, KBN, university.	23rd DEC 2020	
III Internal Assessment Test	11th,12th &13th JAN 2021(Thu, Fri & Sat-Offline)	
Webinar on **Introduction to Remote Sensing & Image Processing by** Dr. P. M Shivakumar Swamy Professor, JSSTE, Bangalore	12th JAN 2021	
Last date for sending IA Marks (SMS)	23rd JAN 2021	
PG **Freshers's Day & Inaugural** Function	23rd JAN 2021	
Parents Meet	25th JAN 2021	
Webinar on **Interpersonal Skills** by Ms. Sonu Prakash Chand, Manager IT Solutions, Eli Lily & Company	25th JAN 2021	
Quiz on **Intellectual Property Rights**	27th JAN 2021	
External NBA Audit By on Mrs. Sowmyashree M.S, BMSIT, Bengaluru	29th JAN 2021	
Internal NBA Audit	19th FEB 2021	
IEEE VTools webinar titled **"Automation in Electronics Engineering"** jointly organized by IEEE Bangalore Section, RYMEC Ballari, by Ramachandra Gambheer Member of IEEE, Western USA	28th FEB 2021	
Webinar on **"Academic and Administrative Audit Process "** under EDP in association with IQAC	4th March 2021	

Dr. T. Hanumantha Reddy & Dr. Veeragangadhar Swamy .		
External Academic Audit (IQAC-NAAC) Dr. Prakash M Prof, SDM Engineering College, Dharwad .	6th MARCH 2021	
Last Working Day	**16/01/2021**	
Practical Examination	21/01/2021 to 02/02/2021	21/01/2021 to 27/01/2021
Theory Examination	08/02/2021 to 25/03/2021	28/01/2021 to 10/02/2021
Commencement of EVEN Semester	**19/04/2021**	19/02/2021

HOD ECE

Head of the Department.
Electronics & Communication Engg
R. Y. M. Engineering College.
(Formerly Vijayanagar Engg. College)
BELLARY-583 104

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI

DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING

Staff Name: Mr K Phanindra Reddy K	**Sem:** VII A & V A
Course Name: Real Time System **Principles of Communication Systems**	**Course Code:**17EC743 **Course Code:**18EC53

Individual Time Table

DAY	9.30am-10.30am	11.00am- 12.00pm	2.30pm-3.30pm
MON			RTS
TUE			
WED	PCS		
THU	RTS	PCS	
FRI		RTS	PCS
SAT			

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

COURSE PLAN 2020-21 (ODD)

Staff Name: Mr Phanindra Reddy K	**Course Type: Core**	**Sem / Sec: 7/A**
Course Name: Real Time System	**Course Code17EC743**	**Total Number of Lecture Hours: 40**
Max marks: 100(40+60)	**Prerequisites: Operating Systems**	

Sl.No	Module Name	Lecture Hours Required
01	Introduction to Real-Time Systems, Concepts of Computer Control	**8**
02	Computer Hardware Requirements for Real-Time Applications	**8**
03	Languages for Real-Time Applications	**8**
04	Operating Systems	**8**
05	Design of RTS –General Introduction, RTS Development Methodologies	**8**

Sl.No	Date	Time	Topic to be Covered
1	01/09/2020	2:30-3:30	**Module – 1** Historical background
2	04/09/2020	9:30-10:30	Elements of computer control system
3	05/09/2020	11:00-12:00	Elements of computer control system, RTS Definition
4	08/09/2020	2:30-3:30	Classification of Real-time Systems
5	11/09/2020	9:30-10:30	Time constraints
6	12/09/2020	11:00-12:00	Classification of Programs
7	15/09/2020	2:30-3:30	Introduction, Sequence Control, Loop control
8	18/09/2020	9:30-10:30	DDC applications
9	19/09/2020	11:00-12:00	Supervisory control
10	22/09/2020	2:30-3:30	Centralized computer control
11	25/09/2020	9:30-10:30	Hierarchical Systems
12	26/09/2020	11:00-12:00	**Module-2** Introduction, General purpose computer
13	29/09/2020	2:30-3:30	Single chip microcontroller,
14	02/10/2020	9:30-10:30	Specialized processors

15	03/10/2020	11:00-12:00	Process-related Interfaces
16	06/10/2020	2:30-3:30	Data transfer techniques
17	09/10/2020	9:30-10:30	Data transfer techniques
18	10/10/2020	11:00-12:00	Communication, Standard Interface
19	13/10/2020	2:30-3:30	**Module -3** Introduction
20	16/10/2020	9:30-10:30	Syntax layout and readability
21	17/10/2020	11:00-12:00	Declaration and Initialization of Variables and Constants
22	20/10/2020	2:30-3:30	Modularity and Variables, Compilation
23	23/10/2020	9:30-10:30	Data types
24	24/10/2020	11:00-12:00	Control Structure, Exception Handling,
25	27/10/2020	2:30-3:30	Low-level facilities, Co routines
26	30/10/2020	9:30-10:30	Interrupts and Device handling,
27	31/10/2020	11:00-12:00	Concurrency, Real-time support
28	03/11/2020	2:30-3:30	Overview of real-time languages
29	06/11/2020	9:30-10:30	**Module-4** Introduction
30	07/11/2020	11:00-12:00	Real-time multi-tasking OS
31	10/11/2020	2:30-3:30	Scheduling strategies
32	13/11/2020	9:30-10:30	Priority Structures, Task management
33	14/11/2020	11:00-12:00	Scheduler and real-time clock interrupt handles
34	17/11/2020	2:30-3:30	Memory Management,
35	20/11/2020	9:30-10:30	Code sharing, Resource control
36	21/11/2020	11:00-12:00	Task co-operation and communication
37	24/11/2020	2:30-3:30	Mutual exclusion
38	27/11/2020	9:30-10:30	**Module-5** Introduction
39	28/11/2020	11:00-12:00	Specification documentation, Preliminary design,
40	01/12/2020	2:30-3:30	Single-program approach

41	04/12/2020	9:30-10:30	Foreground/background
42	05/12/2020	11:00-12:00	Introduction, Yourdon Methodology
43	08/12/2020	2:30-3:30	Ward and Mellor Method
44	11/12/2020	9:30-10:30	Ward and Mellor Method
45	12/12/2020	11:00-12:00	Hartely and Pirbhai Method
46	15/12/2020	2:30-3:30	Hartely and Pirbhai Method

Teaching and Learning Tools: Blackboard/PowerPoint presentation/webinar/lab

Text Books:

1. **Real-Time Computer Control, by Stuart Bennet, 2nd Edn. Pearson Education. 2008.**

Reference Books:

2. **C.M. Krishna, Kang G. Shin, —Real –Time Systems‖, McGraw – Hill International Editions, 1997.**
3. **Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.**
4. **Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005**

Digital Library/E-Resources:

1. 192.168.8.8:8080 Academic Resources
2. 192.168.8.8:8081 Non-Academic Resources
3. 192.168.8.4 - NPTEL/VTU E-learning – Videos

Note: Planning of syllabus is done as per VTU curriculum

Staff Signature

HOD

Rao Bahadur .Y. Mahabaleshwarappa Engineering College Bellary

Dept ECE	2020 - 2021	Title: Report on Syllabus Status

REPORT ON SYLLABUS STATUS

Semester	Branch	Subject	Section	Name of the Staff
7th	ECE	RTS	A	Phanindra Reddy JS

Sl.No	Date	Period	Topics Covered	Remarks
1	3/9/20	1st	M-1 Introduction	
2	4/9/20	2nd	History & Elements of comp. control	
3	18/9/20	2nd	classification of RTS, Programs	
4	21/9/20	3rd	computer control	
5	22/9/20	1st	loop control	
6	25/9/20	2nd	Supervisor control, Centralized comp. control	
7	28/9/20	3rd	M-2 Computer HW requirements for RTS	
8	1/10/20	1st	process Related Interface	
9	5/10/20	3rd	Data transfer techniques	
10	8/10/20	1st	Interrupt	
11	9/10/20	2nd	communication	
12	12/10/20	2nd	Standard Interface	
13	15/10/20	1st	Interfaces	
14	22/10/20	1st	M-4 RTOS	
15	23/10/20	2nd	Scheduling Strategies	
16	29/10/20	3rd	Task Management	
17	5/11/20	1st	Memory management & code sharing	
18	6/11/20	2nd	I/O Subsystems	
19	9/11/20	2nd	M-3 Multitasking Scheduling	
20	12/11/20	3rd	priority based Task mgmt, Scheduling	
21	13/11/20	1th	clock interrupt, mem. mgmt, code sharing	
22	18/11/20	3rd	Resource sharing, Task - cooperation & communication	
23	23/11/20	3rd	mutual exclusion	
24	24/11/20	3rd	M-5 Introduction to design of RTOS	
25	25/11/20	1st	Semaphore & monitor	
26	28/11/20	2nd	RTS development methodology	
27	30/11/20	3rd	cont.. methodology	
28	1/12/20	2nd	Dijkgraaf & Wald miller method	
29	2/12/20	3rd	Yourdon methodology	

Signature
Staff in-charge

Signature
Head of the Department

Rao Bahadur .Y. Mahabaleshwarappa Engineering College Bellary

Dept ECE	2021 - 2021	Title: Report on Syllabus S tatus

REPORT ON SYLLABUS STATUS

Semester	Branch	Subject	Section	Name of the Staff
7	ECE	RTS	A	Phanindra Reddy .B

Sl.No	Date	Period	Topics Covered	Remarks
	3/12/20	3rd	Word & multiple methods	
	7/12/20	3rd	cont. word & multiple	
	9/12/20	3rd	Interrupts & device handling	
	10/12/20	2nd	concurrency & Real time Kernels	
	18/12/20	3rd	overview of Real time Languages	
	19/12/20	1st	Revision on M-1 classification Spectrum	
	30/12/20	3rd	contd. components Hierarchy	
	1/1/21	2nd	M-2 General purpose computer	
	4/1/21	1st	Data transfer, Synchronization	
	5/1/21	3rd	M-4 Scheduling Memory mgmt	
	6/1/21	2nd	sharing, Methodologies	

Signature
Staff In-charge

Signature
Head of the Department

COURSE EVALUATION AND ASSESSMENT SCHEME-2017

	What		To Whom	When/ Where (Frequency in the course)	Max Marks	Evidence Collected
Direct Assessment Methods	IA	Internal Assessment Tests	Students	Thrice(Average of three IA Tests)	30	Blue Books
		Assignment		Thrice(Before IA Test and average of 3 is taken)	10	Assignment Books
		Practical Assessment		Once	40	Practical evaluation
	FE	Final Examination		End of Course (Answering One of two questions from five Modules)	100	Result sheet
		Practical Examination		One question from lot	100	Result sheet
Indirect Assessment Methods	Students Feedback		Students	End of the course	-	Questionnaire
	Course Exit Survey					

Questions for IA and FE will be designed to evaluate the various educational components (Bloom's taxonomy)

REAL TIME SYSTEMS

B.E., VII Semester, Electronics & Communication Engineering /Telecommunication Engineering

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**17EC743**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

Credits – 03

Course Objectives: This Course will enable students to:

- Discuss the historical background of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Module-1

Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.

Concepts of Computer Control: Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. (Text Book: 1.1 to 1.6 and 2.1 to 2.6) **L1, L2**

Module-2

Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.(Text Book: 3.1 to 3.8) **L1, L2**

Module-3

Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. (Text Book: 5.1 to 5.14) **L1, L2, L3**

Module-4

Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.(Text Book: 6.1 to 6.11) **L1, L2**

Module-5

Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System.

RTS Development Methodologies: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method. (Text Book: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5) **L1, L2, L3**

Course Outcomes: At the end of the course, students should be able to:

- Understand the fundamentals of Real time systems and its classifications.
- Understand the concepts of computer control, operating system and the suitable computer hardware requirements for real-time applications.
- Develop the software languages to meet Real time applications.
- Apply suitable methodologies to design and develop Real-Time Systems.

Text Book:

Real-Time Computer Control, by Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. C.M. Krishna, Kang G. Shin, "Real –Time Systems", McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
Assignment-I (20-21 Odd Sem)

Staff Name: MrK Panindra Reddy/ Mr Channaveerana Gouda	**Sem:VII** A/B
Course Name:Real Time System	**Course Code:**17EC743
Max marks: 10	**Prerequisites:** Operating System

Q No	QUESTIONS	BTL	CO	PO
Q1	Explain different LAN topologies	L2	1	1
Q2	Write a note on Hierarchical system	L2	1	1
Q3	Explain Different type of programs in system design	L1 L2	1	1
Q4	Describe a) Batch process b) Continuous process c)Laboratory	L2	1	1
Q5	Explain different forms of parallel computer architecture	L2	2	1
Q6	a) Define Real Time System. b) Sketch computer control system showing hardware , software & communication interface and explain	L1	1	1
Q7	Explain working principle of daisy chain interrupt structure with diagram	L2	2	2
Q8	Explain basic interrupt input mechanism with diagram and flowchart	L2	2	1
Q9	Explain the Time constraints with examples	L2	2	1
Q10	Explain analog input and output interface with diagram	L2	2	2
Q11	Explain the concept of Sequence Control	L2	1	1
Q12	Explain the concept of centralized computer concept	L2	1	1

Signature of faculty

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
CONTINIOUS INTERNAL EVALUATION-I (20-21Odd Sem)

Staff Name: Mr. KhajaMoinuddin / MrK Phanindra Reddy	**Sem:VII** A/B	**Date:** 18/10/2020
Course Name:Real Time System	**Course Code:**17EC743	**Time : 2.30-4.00 PM**
Max marks: 50	**Prerequisites:** Operating System	**Total Contact Hours :** 40

NOTE:Answer five questions (at least one from each pair of questions)

Q No	QUESTIONS	Marks	BTL	CO	PO	PSO
Q1	Explain the Time constraints with examples	10	L2	1	1	
	OR					
Q2	Explain Different type of programs in system design	10	L2	1	1	
Q3	a) Define Real Time System. b) Sketch computer control system showing hardware , software & communication interface and explain	10	L1 L2	1	1	
	OR					
Q4	Describe a) Batch process b) Continuous process c)Laboratory	10	L2	1	1	
Q5	Explain different forms of parallel computer architecture	10	L2	2	1	
	OR					
Q6	Write a note on Hierarchical system	10	L1	1	1	
Q7	Explain working principle of daisy chain interrupt structure with diagram	10	L2	2	2	
	OR					
Q8	Explain basic interrupt input mechanism with diagram and flowchart	10	L2	2	1	
Q9	Explain different LAN topologies	10	L2	2	1	
	OR					
Q10	Explain analog input and output interface with diagram	10	L2	2	2	

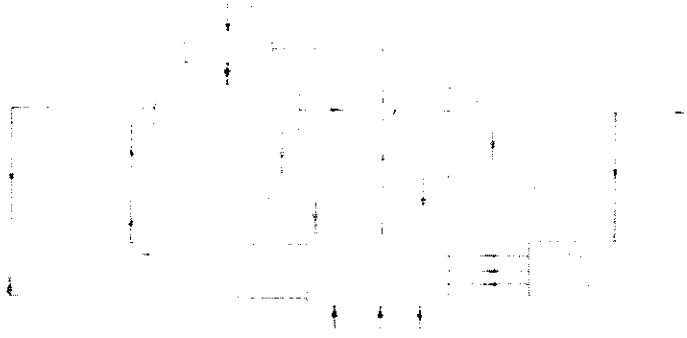
IA Co-ordinator

Signature of faculty

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
SCHEME OF EVALUATION-I(20-21 Odd Sem)

Staff Name: Mr. KhajaMoinuddin / K Phanindra Reddy/ Channaveerana Gouda	**Sem:VII** A/B	**Date:** 18/10/2020
Course Name:Real Time System	**Course Code:**17EC743	**Time : 2.30-4.00 PM**
Max marks: 50	**Prerequisites:** Operating System	**Total Contact Hours :** 40

Q No	Solution	Marks
Q1	Real time systems are divided into two categories: 1. Hard real-time: these are systems that must satisfy the deadlines on each and everyoccasion. 2. Soft real-time: these are systems for which an occasional failure tomeet a deadline does not comprise the correctness of thesystem. An automatic bank teller provides an example of a system with a soft time constraint. A typical system is event initiated in that it is started by the customer placing their card in the machine	
Q2	Three types ofprogramming: 1.Sequential; 2.Multi-tasking;and 3. Real-time. SEQUENTIAL: MULTI-TASKING: REAL-TIME:	
Q3		

Q4

PROCESS:

BATCH

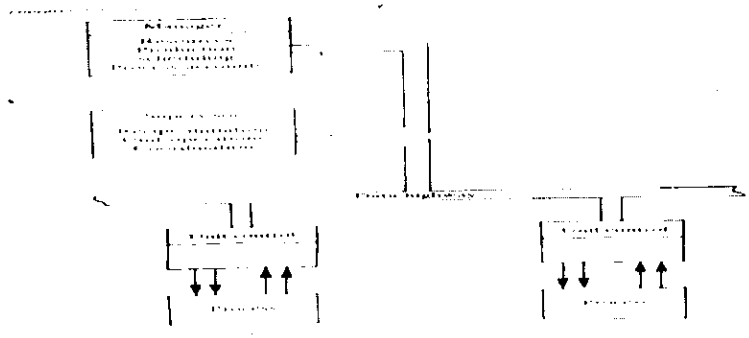
Thetermbatchisusedtodescribeprocessesinwhichasequenceofoperationsiscarried out to produce a quantity of a product - the batch - and in which the sequence is then repeated to produce further batches. The specification of the product or the exact composition may be changed between the differentruns.

CONTINUOUS: The term *continuous* is used for systems in which production is maintained fo long periods of time without interruption, typically over several months or even years. An example of a continuous system is the catalytic cracking of oil in which the crude oil enters a end and the various products - fractionates – are removed as the process continues. The rat the different fractions can be changed but this is done without halting theprocess.

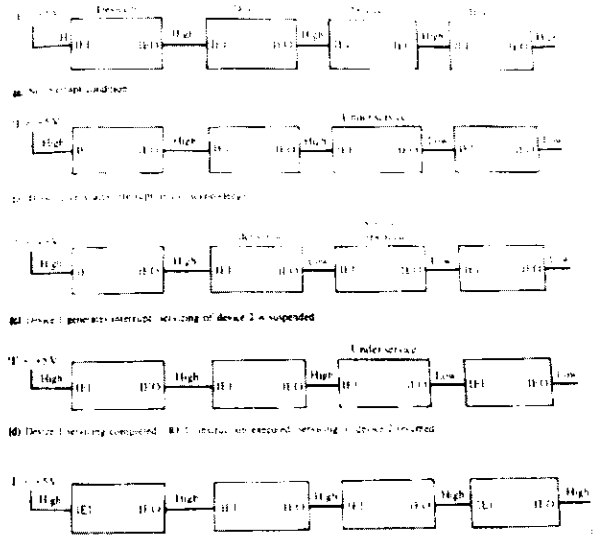
LABORATORY SYSTEMS: Laboratory-based systems are frequently of the operator-initiated t in that the computer is used to control some complex experimental test or some complex equipment used for routine testing. A typical example is the control and analysis of data fro vapor phase chromatograph.

Q5

Q6

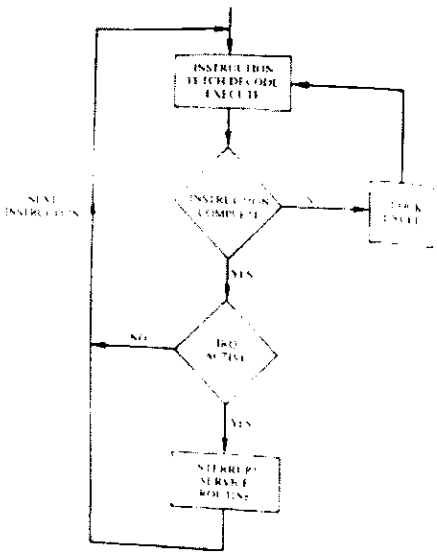


Q7



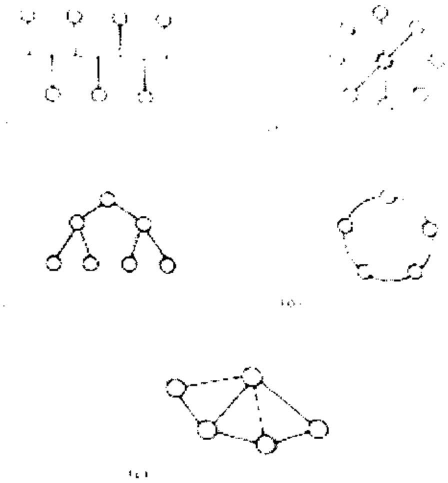
A frequently used arrangement is the daisy chain in which an 'acknowledge' signal is propagated through the devices until it is blocked by the interrupting device Figure 3.15 shows a typical arrangement. Each unit has an IEI (Interrupt Enable In) pin and an IEO (Interrupt Enable Out) pin; it is assumed that on both pins the active signal is high. The first IEI in the chain is set permanently on 'high'. For any given

Q8



```
INIT:  CALL SAVREG  ;SAVREG is routine which saves
                    ;working registers
;
;code for interrupt handling is inserted here
;
       CALL RESREG  ;RESREG is routine which
                    ;restores working registers
       EI           ;enable interrupts
       RETI         ;return from interrupt routine
```

Q9



[illegible] The system has many of the characteristics of the star but [illegible] [illegible] The system has many of the nodes have to act as [illegible] of [illegible] central switching node, many of the nodes have to act as switches [illegible] [illegible] it can closely reflect the actual structure of the application. [illegible] [illegible] of new nodes to a tree [illegible] can be difficult.

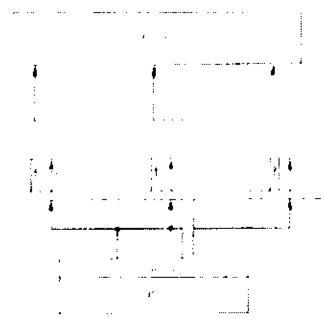
[illegible] It is probably the most popular method. The ring is typically [illegible] [illegible] transmission system, that is the ring itself contains regeneration circuits which amplify the signals. The information placed on a ring network continues to circulate until a device removes it from the ring. In some systems the originating device removes the data from the ring. The information is broadcast in the sense that it is available to all devices connected to the ring.

Mesh: The mesh topology allows for random interconnection between the various nodes. It provides a means by which alternative routes between nodes can be found and hence has built into it a form of redundancy. A problem [illegible] can arise with the mesh is that there can be a variable delay [illegible]

This is the simplest of all the LAN topologies. The bus is normally passive and all the devices are simply plugged into the transmitting medium. The bus is inherently reliable because of its passive nature but there may be a limitation on the length of a bus in that any transmitting device connected has to be able to transmit for the full length of the bus. It is a broadcast system and hence a packet of data placed on the bus is available to all devices.

Star: The star network is not very widely used, it depends on a central switching node to which all other nodes are connected by a bidirectional link. Data sent to the central switch can be forwarded either in the broadcast mode, that is to all other nodes, or only to a specified node. The computer-controlled PABX (Private Automatic Branch eXchanges) used in many businesses operate in the star mode — all the telephone lines connect to the central unit while the forwarding system used is to a specified node. A weakness of the

Q10



IA Co-ordinator

C.C.
Electronics & Communication Engg
RYMEC, Ballari

Signatureoffaculty

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BELLARY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Sub: RTS (17EC743) **Sem/Sec: 7 A** **2020-21**

IA-1 PERFORMANCE ANALYSIS

Internal Assessment 1

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
CO mapping	CO1	CO1	CO1	CO1	CO2	CO1	CO2	CO2	CO2	CO2
Max Marks /Question	10	10	10	10	10	10	10	10	10	10
Total marks of class /question	180	180	10	350	100	260	40	320	300	60
No. of students attended	18	18	1	35	10	26	4	32	30	6
No of students scored > 65% of marks/Question	18	18	1	35	10	26	4	32	30	6
Percentage 0f 65% marks scored	100	100	100	100	100	100	100	100	100	100

Mark range	0-10	11 to 20	21 to 30	31-40	41-50
No. Of Students					36

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
Assignment-II (20-21 Odd Sem)

Staff Name: MrK Panindra Reddy/ Mr Channaveerana Gouda	**Sem:VII** A/B
Course Name:Real Time System	**Course Code:**17EC743
Max marks: 10	**Prerequisites:** Operating System

Q No	QUESTIONS	BTL	CO	PO
Q1	Sketch typical structure of real time operating system and explain	L3	4	1
Q2	Explain the general structure of Input Output Sub System(IOSS)	L2	4	1
Q3	List the functions of task management. Explain task state diagram and task state	L1 L2	4	1
Q4	Explain two scheduling Strategies	L1 L2	4	2
Q5	Sketch general structure of real time operating system and explain	L2	4	2
Q6	Explain a)Task chaining & swapping b)Task overlaying	L2	4	2
Q7	Explain A) Portioned memory B) Non- Portioned memory	L1 L2	4	1
Q8	What is binary semaphore? Describe function of binary semaphore by considering a task wishes to access a printer	L2	4	1
Q9	Write a note on Mutual Exclusion	L2	4	1
Q10	What is code sharing? Discuss how problems of code sharing is overcome by using different methods	L2	4	1
Q11	Describe software design for RTS using software modules	L2	5	2
Q12	Describe hardware design in case of preliminary design of RTS	L2	5	2
Q13	Sketch the flow chart & Explain foreground/background approach	L2	5	2
Q14	With neat flow-chart describe single program approach with reference to RTS design	L1	5	1
Q15	Explain planning and development phase in designing of Real time system	L1	5	2

Signature of faculty

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
CONTINIOUS INTERNAL EVALUATION -II(20-21 Odd Sem)

Staff Name: Mr K Panindra Reddy/Mr Channaveerana Gouda	**Sem:VII** A/B	**Date:** 03/12/2020
Course Name:Real Time System	**Course Code:**17EC743	**Time : 9.15-10.45AM**
Max marks: 50	**Prerequisites:** Operating System	**Total Contact Hours :** 40

NOTE:Answer five questions (at least one from each pair of questions)

Q No	QUESTIONS	Marks	BTL	CO	PO	PSO
Q1	Sketch typical structure of real time operating system and explain	10	L3	4	1	
	OR					
Q2	Explain two scheduling Strategies	10	L2	4	1	
Q3	List the functions of task management. Explain task state diagram and task state	10	L1 L2	4	1	
	OR					
Q4	What is binary semaphore? Describe function of binary semaphore by considering a task wishes to access a printer with diagram	10	L1 L2	4	2	
Q5	What is code sharing? Discuss how problems of code sharing is overcome by using different methods	10	L2	4	2	
	OR					
Q6	Explain a)Task chaining & swapping b)Task overlaying	10	L2	4	2	
Q7	Describe hardware design in case of preliminary design of RTS	10	L1 L2	5	1	
	OR					
Q8	Explain planning and development phase in designing of Real time system	10	L2	5	1	
Q9	Describe software design for RTS using software modules	10	L2	5	1	
	OR					
Q10	Sketch the flow chart & Explain foreground/background approach	10	L2	5	1	

IA Co-ordinator

C.C.

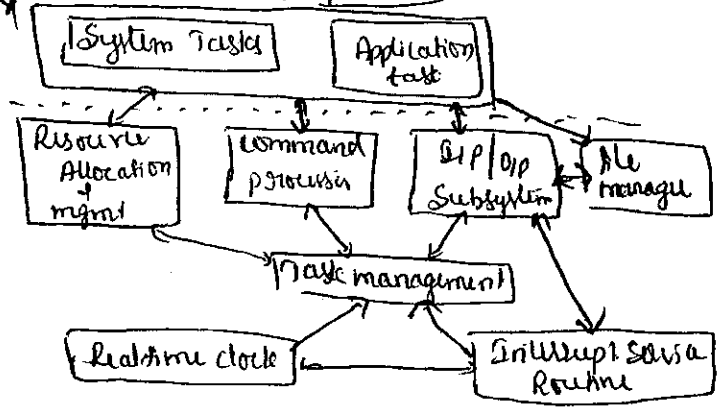
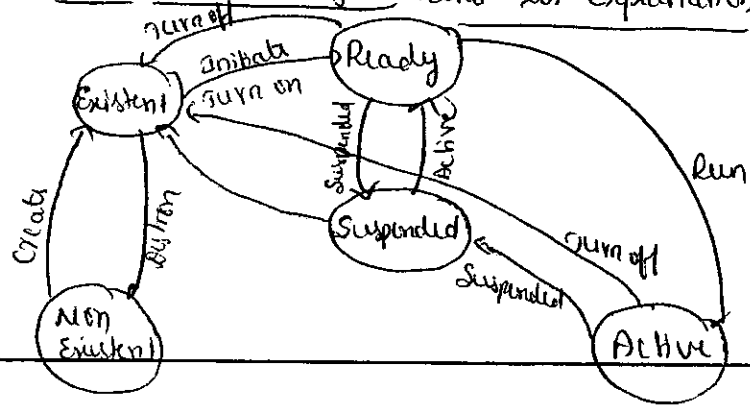
Signature of faculty

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome)PO (Program Outcome)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
SCHEME OF EVALUATION -II(20-21 Odd Sem)

Staff Name: Mr K Panindra Reddy/Mr Channaveerana Gouda	**Sem:VII** A/B	**Date:** 03/12/2020
Course Name:Real Time System	**Course Code:17EC743**	**Time : 9.15-10.45AM**
Max marks:50	**Prerequisites:** Operating System	**Total Contact Hours :** 40

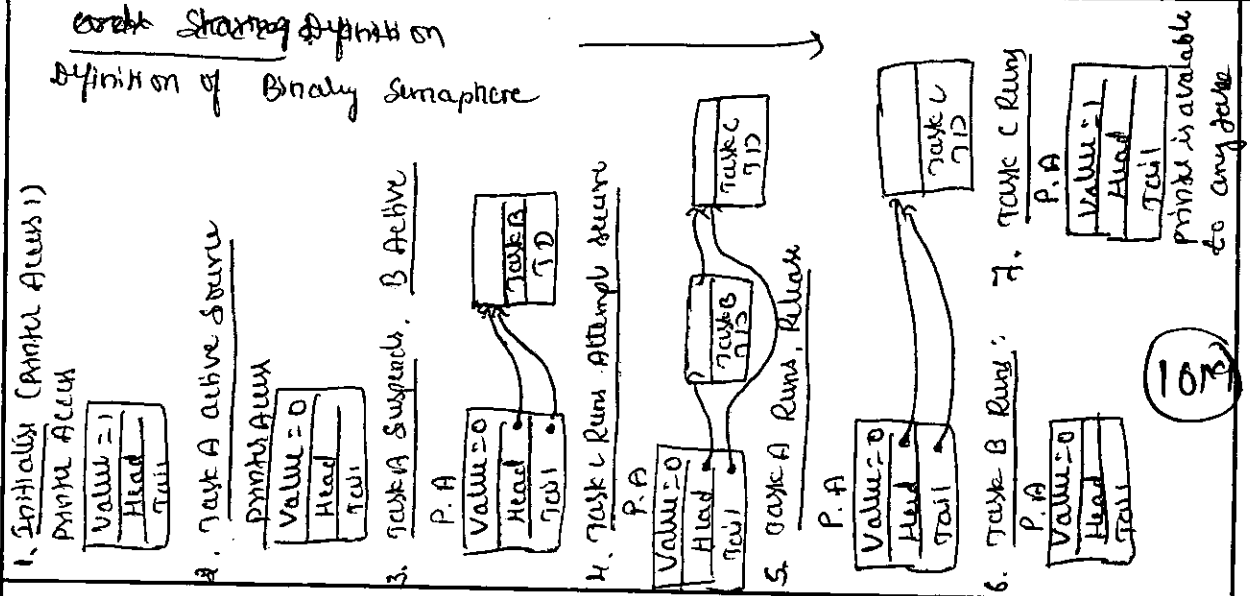
NOTE:Answer five questions (at least one from each pair of questions)

Q No	SOLUTIONS	Marks
Q1	Typical Structure of RTS:  * Explanation on Real time System	6M 4M
Q2	Scheduling Strategies * (1) cyclic Scheduling and its Explanation (2) pre-emptive Scheduling and its Explanation	5M 5M
Q3	* List of functions of Task management * Task State Diagram and its explanation  	5M 5M

Q4

Code Sharing Definition

Definition of Binary Semaphore



10M

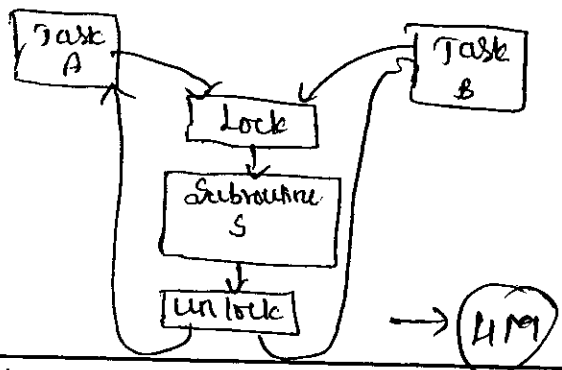
Q5

* Code Sharing:

Definition → 2M

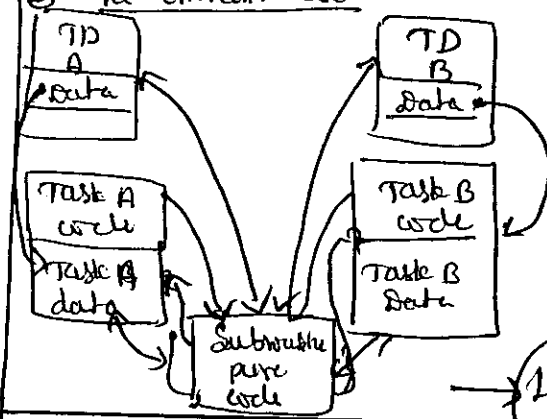
Two methods to Can be used in code sharing to avoid sharing

① Serially Reusable code



→ 4M

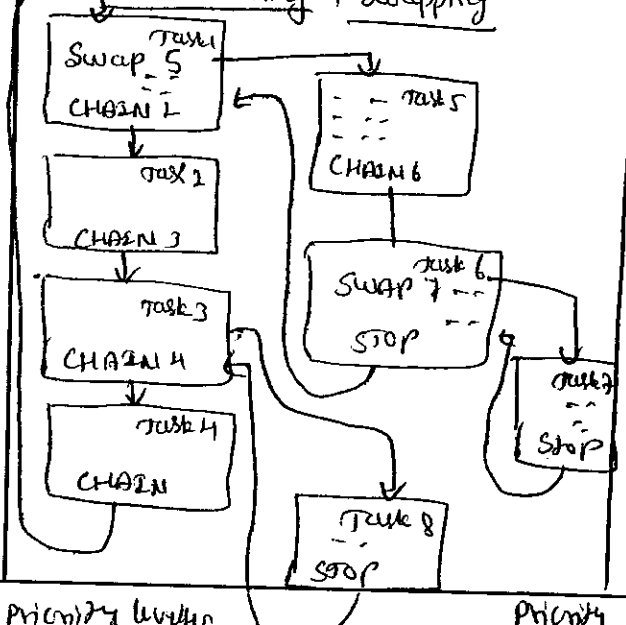
② Re-Entrant code



→ 4M

Q6

A) Task Chaining + Swapping



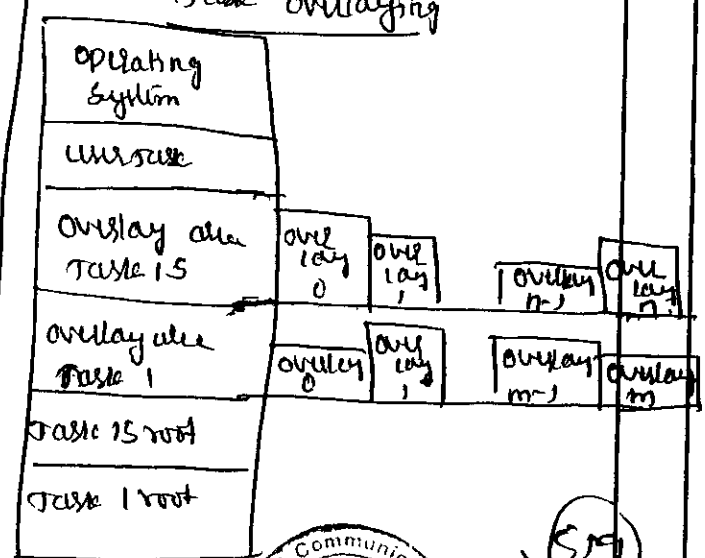
Priority Level 0

Priority Level 1

Priority Level 2

→ 5M

Task Overlaying

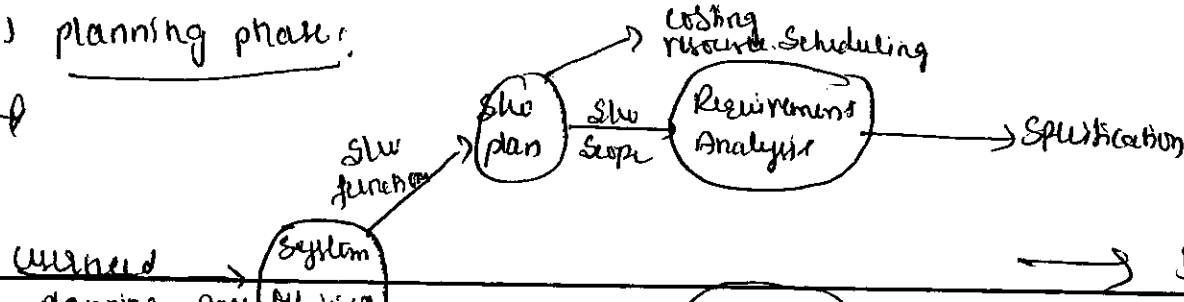


→ 5M

C.C.

07 Discription on Hardware design in case of Preliminary design of Real time System and its Explanation → 10M

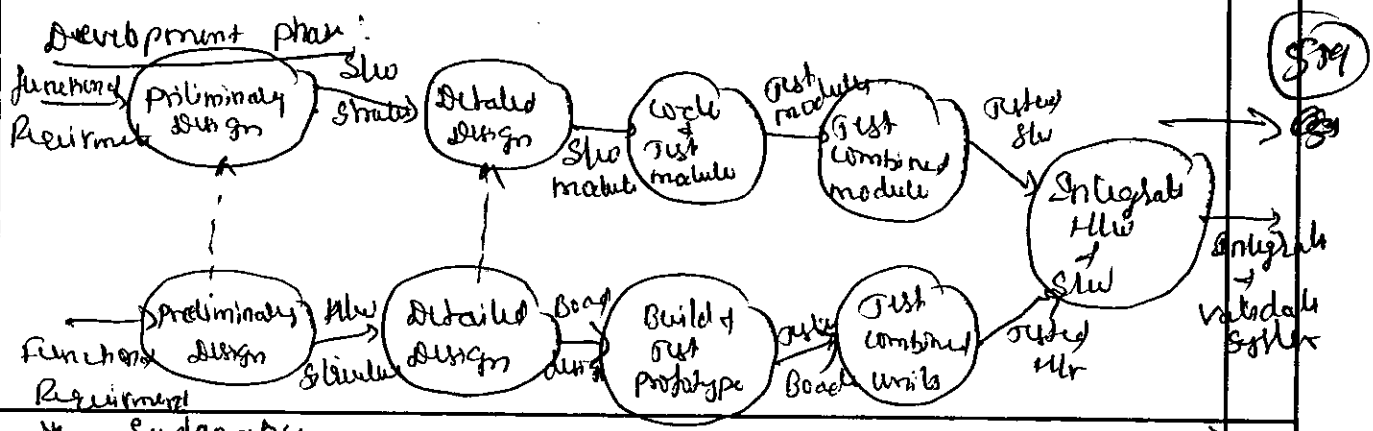
08 (a) planning phase:



→ 5M

Explanation →

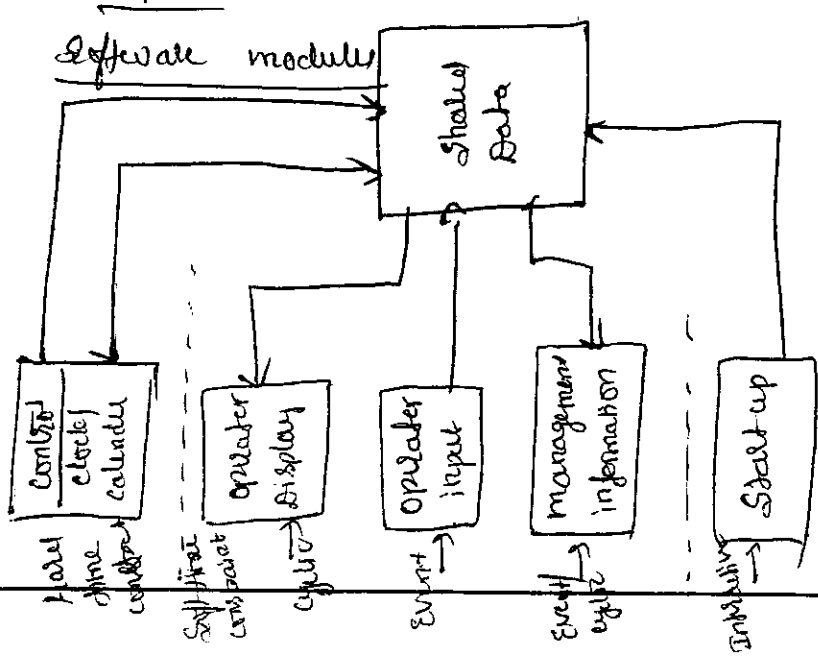
09 Development phase:



→ 5M

Explanation →

09 Software modules

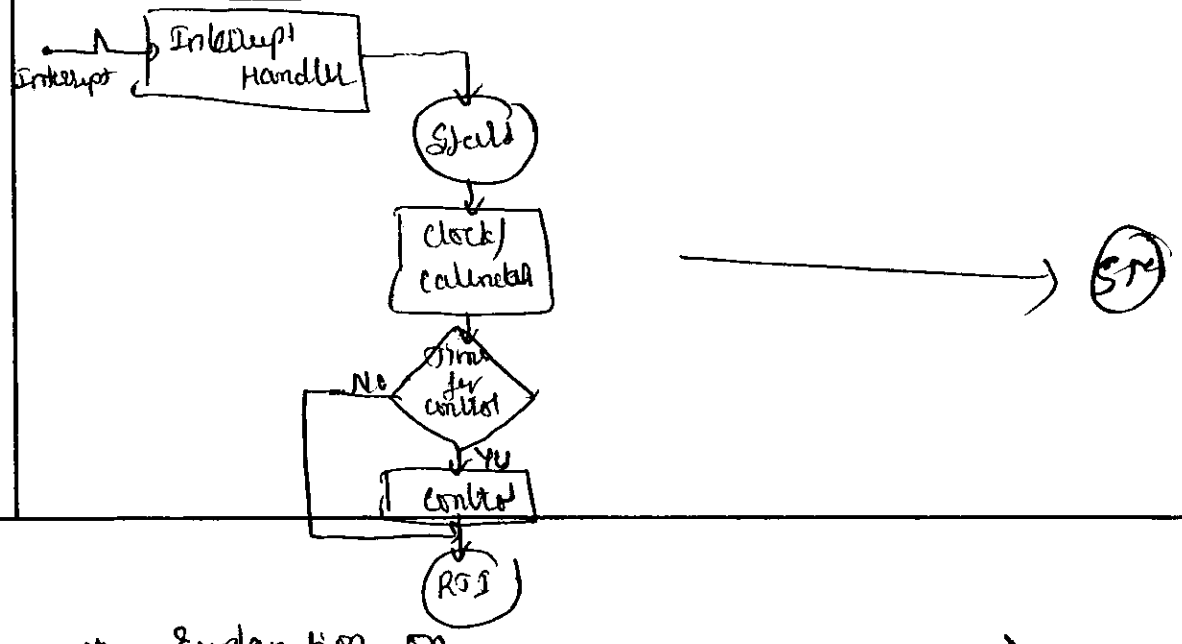


→ 5M

Explanation on Software modules → 4M

Q10

Fore ground Approch :

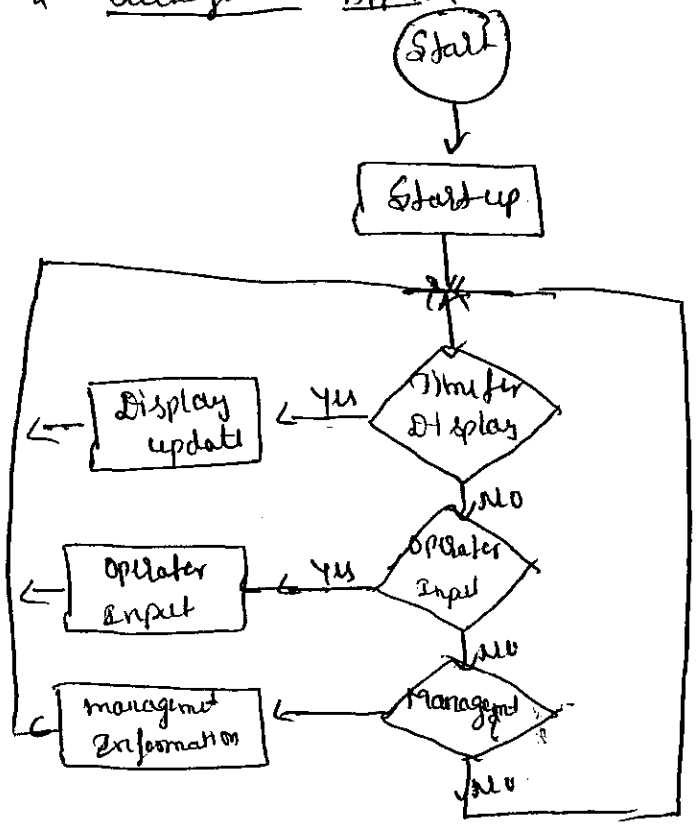


* Explanation on Foreground Approch →

IA Co-ordinator **Signature of faculty**

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome) PO (Program Outcome)

* Background Approch



* Explanation on Background Approch →

IA - Co-ordinator

Sign of faculty

1)

2)

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Sub: RTS (17EC743) **Sem/Sec: 7 A** **2020-21**

IA-1IPERFORMANCE ANALYSIS

Internal Assessment 2

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
CO mapping	CO4	CO4	CO4	CO4	CO4	CO4	CO5	CO5	CO5	CO5
Max Marks /Question	10	10	10	10	10	10	10	10	10	10
Total marks of class /question	280	80	359		80	280	130	240	298	60
No. of students attended	28	8	36		8	28	13	24	30	6
No of students scored > 65% of marks/Question	28	8	36		8	28	13	24	30	6
Percentage 0f 65% marks scored	100	100	100	100	100	100	100	100	100	100

Mark range	0-10	11 to 20	21 to 30	31-40	41-50
No. Of Students					36

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
Assignment-III (20-21 Odd Sem)

Staff Name: MrK Panindra Reddy/ Mr Channaveerana Gouda	**Sem:VII** A/B
Course Name:Real Time System	**Course Code:**17EC743
Max marks: 10	**Prerequisites:** Operating System

Q No	QUESTIONS	BTL	CO	PO
Q1	List and explain in brief the six requirements for a real time programming language.	L1 L2	3	1
Q2	Explain exceptional handling with a simple example pseudo code.	L2	3	1
Q3	Describe the basic form of concurrency through the coroutines with a simple pseudo code.	L2	3	1
Q4	Illustrate the function of interrupts and device handling with a simple pseudo code.	L2	3	2
Q5	Explain the run-time support mechanisms implemented by a real time programming language.	L2	3	2
Q6	Explain the following control structures a) Repeat…until b) while c)if d) if…then…else	L2	3	2
Q7	Sketch and explain the flow chart for software modeling in RTS development methodology.	L1 L2	5	1
Q8	Outline the abstract modeling approach of Ward and Miller method with a neat diagram.	L2	5	1
Q9	Describe the context diagram for a drying oven with a neat diagram.	L2	5	1
Q10	Explain the control specification (CSPEC) with state transition diagram and state transition matrix.	L2	5	1
Q11	Describe hardware design in case of preliminary design of RTS	L2	5	2
Q12	Explain planning and development phase in designing of Real time system	L1	5	2

Signature of faculty

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
CONTINIOUS INTERNAL EVALUATION -III(20-21 Odd Sem)

Staff Name: Mr K Phanindra Reddy. K / Mr Channaveerana Gouda	**Sem:VII** A/B	Date: 04/01/2021
Course Name:Real Time System	**Course Code:**17EC743	Time : 10.00-11.30AM
Max marks: 50	**Prerequisites:** Operating System	Total Contact Hours : 40

NOTE:Answer five questions (at least one from each pair of questions)

Q No	QUESTIONS	Marks	BTL	CO	PO	PSO
Q1	List and explain in brief the six requirements for a real time programming language.	10	L1 L2	3	1	
	OR					
Q2	Explain exceptional handling with a simple example pseudo code.	10	L2	3	2	
Q3	Describe the basic form of concurrency through the coroutines with a simple pseudo code.	10	L2	3	1	
	OR					
Q4	Illustrate the function of interrupts and device handling with a simple pseudo code.	10	L2	3	2	
Q5	Explain the run-time support mechanisms implemented by a real time programming language.	10	L2	3	2	
	OR					
Q6	Explain the following control structures a) Repeat…until b) while c)if d) if…then…else	10	L2	3	2	
Q7	Sketch and explain the flow chart for software modeling in RTS development methodology.	10	L1 L2	5	1	
	OR					
Q8	Outline the abstract modeling approach of Ward and Miller method with a neat diagram.	10	L2	5	2	
Q9	Describe the context diagram for a drying oven with a neat diagram.	10	L2	5	1	
	OR					
Q10	Explain the control specification (CSPEC) with state transition diagram and state transition matrix.	10	L2	5	2	

IA Co-ordinator

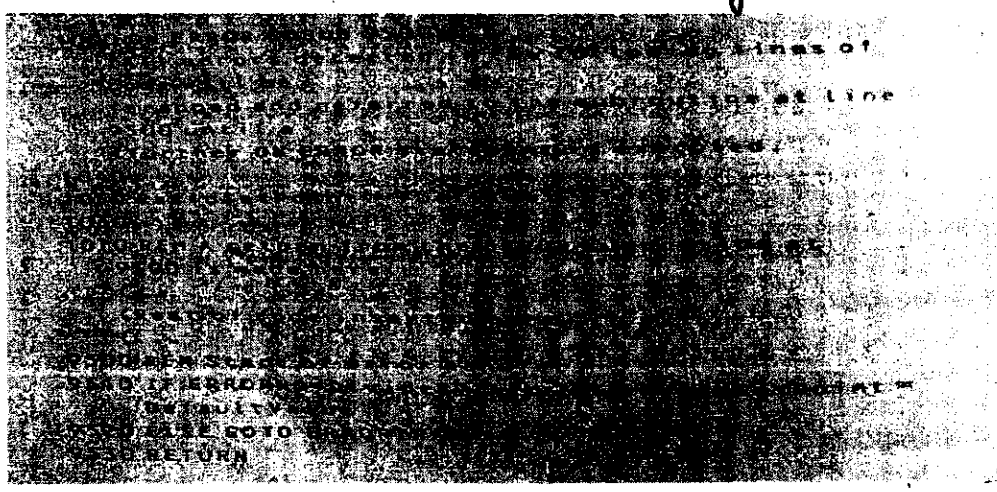
C.C.

Signature of faculty

Note: BTL (Blooms Taxonomy Level) CO (Course Outcome)PO (Program Outcome)

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
DEPARTMENT OF ELECTRONICS &COMMUNICATIONENGINEERING
SCHEME OF EVALUATION-III(20-21 Odd Sem)

Staff Name: Mr K Phanindra Reddy. K / Mr Channaveerana Gouda	**Sem:VII** A/B	**Date:** 04/01/2021
Course Name:Real Time System	**Course Code:**17EC743	**Time : 10.00-11.30AM**
Max marks: 50	**Prerequisites:** Operating System	**Total Contact Hours :** 40

Q No	Solution	Marks
Q1	Six Requirments for a Real time programming Language ① Security ② Readbility ③ Flexibity ④ Simplicity ⑤ Portability ⑥ Efficiency → Explanation on Each Requirments ⟶	3M ⑤ 3M 7M
Q2	pseudo code on Exception Handling  → 6M → Explanation on Exceptional handling →	4M
Q3	→ Explanation on concurency through coroutines ⟶	4M

In Modula-2 the basic form of concurrency is provided by coroutines. The procedures NEWPROCESS and TRANSFER exported by SYSTEM are defined as follows:

```
PROCEDURE NEWPROCESS(parameterlessProcedure:PROC;
                     workspaceAddress:ADDRESS;
                     workspaceSize:CARDINAL;
                     VAR coroutineNet:ADDRESS (* PROCESS *));

PROCEDURE TRANSFER(VAR source, destination : ADDRESS
                   (*PROCESS*));
```

→ 6M

pseudo code on Coroutine

Q4

```
IOTRANSFER (VAR interruptHandler, interruptedProcess : PROCESS;
            interruptVector : CARDINAL)
```

The action of IOTRANSFER is to save the current status of interruptHandler and to resume execution of interruptedProcess, that is to wait for an interrupt. When an interrupt occurs the equivalent of a

```
TRANSFER (interruptedProcess, interruptHandler)
```

occurs. A skeleton interrupt handler would thus take the form

```
BEGIN
  LOOP
    IOTRANSFER (interruptHandler, interruptedProcess,
interruptVector);
(* interrupt handler waits at this point for interrupt *)
  END LOOP
END;
```

→ 6M

Explanation on interrupts and device handling → 4M

Q5

Run time Support

- Explanation on Run time Support
- Example on checking on array bounds.
- Two way to do array checking
  - (a) array[i] → 'i' is an integer $1 \leq i \leq 20$
  - (b) Insert check before every array access

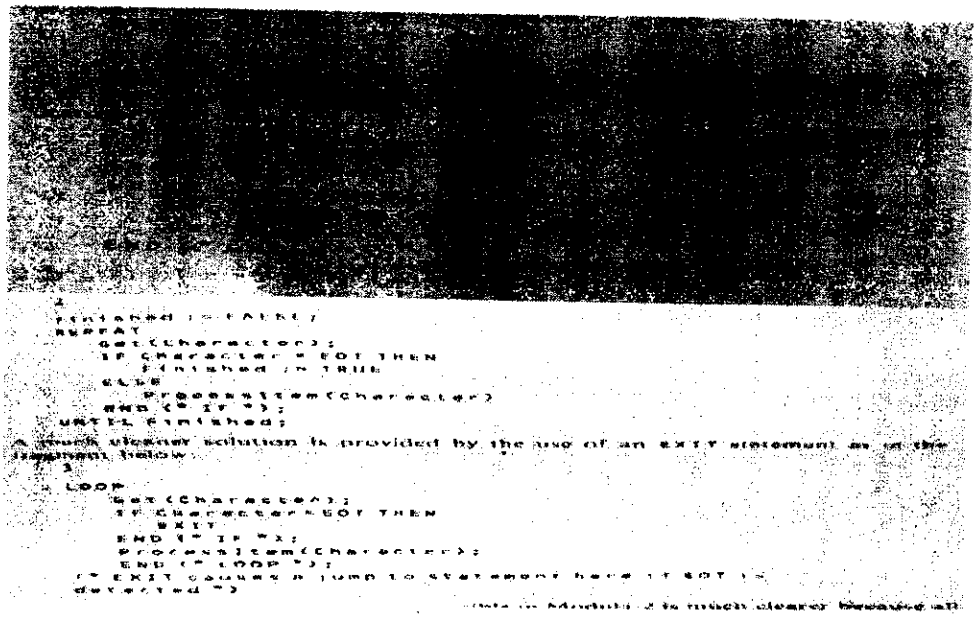
→ 10M

Q6

writing Syntax format for

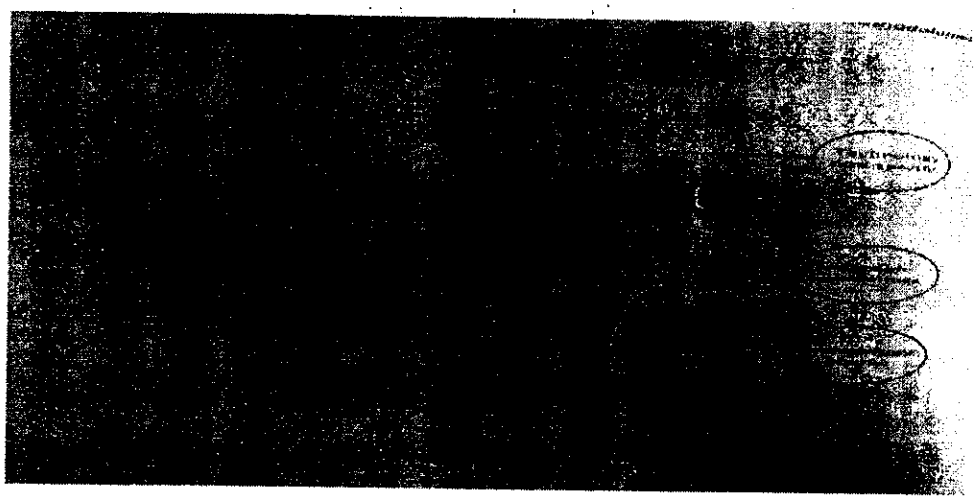
(i) Repeat...until (ii) while

(iii) if (iv) if...then...else



→ 10M

Q7

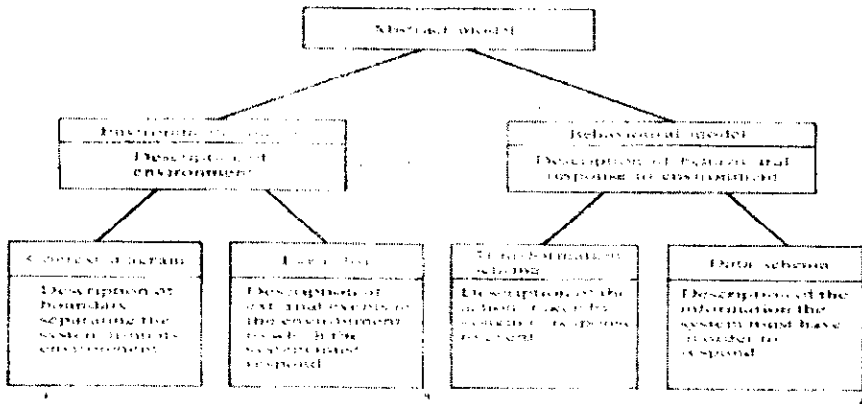


→ 4M

Explanation on Software modeling flow chart
And Each block and i) Requirement capture & analysis
ii) Design (iii) Realisation

→ 6M

Q8



→ 4M

Explanation on
(i) Abstract model
(ii) Environment model and its Subblock
(iii) Behavioral model and its Subblock → 6M

Q9

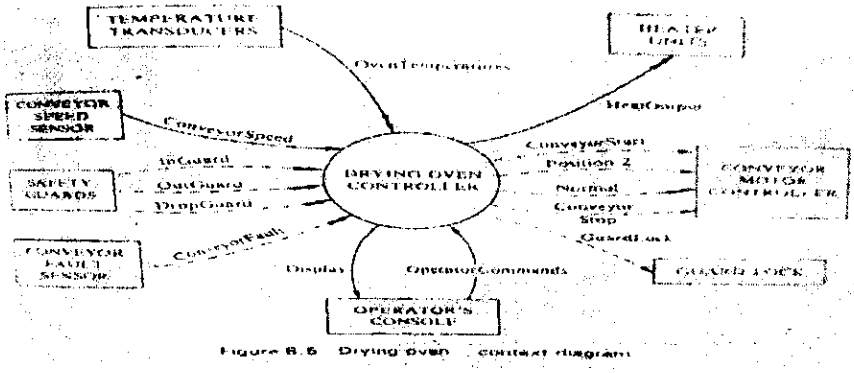
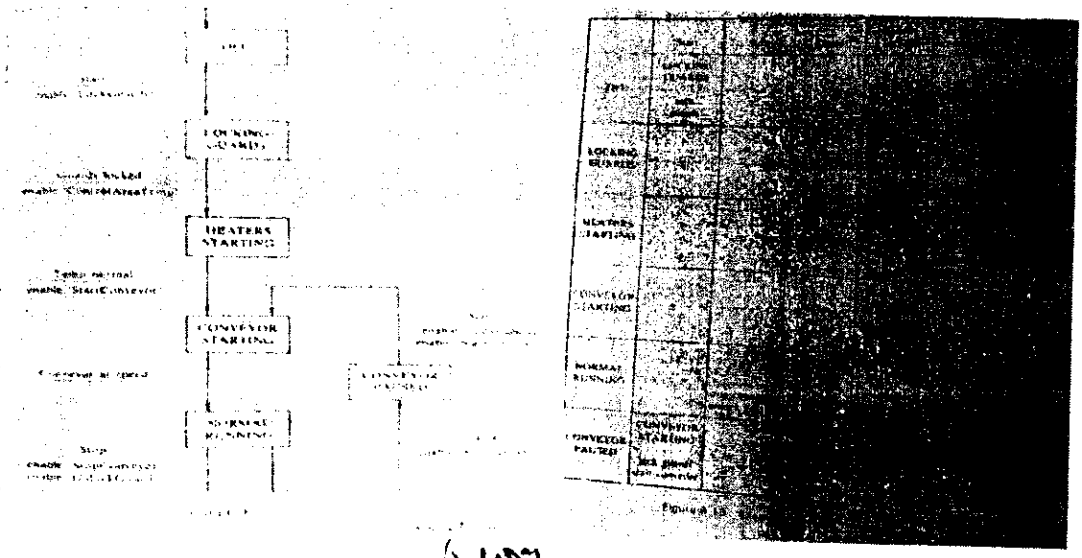


Figure 8.5 Drying oven context diagram

→ 5M

Explanation on notation of control & data flow
——→ continuous data ——→ Discrete data
- - -→ continuous control ——- -→ Discrete control → 5M

Q10



→ 4M → 4M

18M

Explanation on STM and STD → 2M

IA Co-ordinator

C.C.

Signature of faculty

RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BELLARY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Sub: RTS (17EC743) **Sem/Sec: 7 A** **2020-21**

IA-1)PERFORMANCE ANALYSIS

Internal Assessment 3

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
CO mapping	CO3	CO3	CO3	CO3	CO3	CO3	CO5	CO5	CO5	CO5
Max Marks /Question	10	10	10	10	10	10	10	10	10	10
Total marks of class /question	10	10	10	10	10	10	10	10	10	10
No. of students attended	254	72	215	78	228	80	45	295	90	234
No of students scored > 65% of marks/Question	28	8	26	9	29	10	5	32	11	25
Percentage 0f 65% marks scored	85	100	80	88	79	80	80	93	81	92

Mark range	0-10	11 to 20	21 to 30	31-40	41-50
No. Of Students			1	8	27

Faculty: Phanindra Reddy K

Course Name: Real Time Systems

Course Code: 17EC743

Academic Year: 2020-21

CIE/SEE Marks

Sl. No	USN NO	NAME	CIE	SEE	Total
1	3VC16EC011	MONISHA B S	37	28	65
2	3VC16EC033	HARITHA	36	33	69
3	3VC16EC065	RAGHAVENDRA	38	21	59
4	3VC16EC098	UDAY GEETH RAJ	37	40	77
5	3VC17EC004	ANJUM K M	40	39	79
6	3VC17EC009	BHAVANI	40	51	91
7	3VC17EC015	CHETANA GUMASTE	40	38	77
8	3VC17EC016	DIVYASHREE	39	34	74
9	3VC17EC018	GAGANA B J	40	35	74
10	3VC17EC022	JAIPRAKASH N	39	41	80
11	3VC17EC023	JYOTHI H	39	32	72
12	3VC17EC024	K SUSHMA	40	39	79
13	3VC17EC025	K SWETHA	40	34	74
14	3VC17EC027	KEERTHI M V	40	41	81
15	3VC17EC031	MANASA B	40	38	78
16	3VC17EC033	MANJUNATH SUNKAD	39	36	75
17	3VC17EC035	MEGHANA R	40	41	81
18	3VC17EC036	N SOWBAGYASHREE	40	32	72
19	3VC17EC038	NAYUM PASHA	38	29	67
20	3VC17EC039	NEELESH PATIL	37	39	76
21	3VC17EC044	PAWAN KUMAR M	39	35	74
22	3VC17EC047	PRAVEEN KUMAR GOTUR	38	40	78
23	3VC17EC050	RAJASHEKAR REDDY S	38	36	74
24	3VC17EC051	RAJU GHEEWARI	40	30	70
25	3VC17EC055	S KIRAN KUMAR	39	41	80
26	3VC17EC060	SAI KRISHNA BURUGUPALL	38	34	72
27	3VC17EC061	SAI KRISHNA M	40	34	74
28	3VC17EC062	SEEMA P	40	50	90

Sl. No	USN NO	NAME	CIE	SEE	Total
29	3VC17EC069	SONIA	40	36	76
30	3VC17EC071	SOUNDARYA V S	40	51	91
31	3VC17EC073	M SUCHITHA	40	47	87
32	3VC17EC076	TEJASHWINI M	39	36	75
33	3VC17EC078	TRIVENI	40	39	79
34	3VC17EC079	VENKATESH K	38	39	77
35	3VC17EC081	VINAYAKA V	39	36	75
36	3VC18EC402	RAGHAVENDRA KM	40	35	75
37					
38					
39					
40					
41					
42					
43					
44					
64					
65					
Number of students scoring >= 27 in EXTERNAL				**35**	

EXTERNAL EXAM

Number of students appeared for the exam	**36**		-
Number of students scoring >= 45% in EXTERNAL	**35**		-
Percentage	**0.97**		-
Achieved target:	97%		
ATTAINMENT LEVEL	3		

Assignment Marks 2020-21

Faculty: Phanindra Reddy K

Course Name: Real Time Systems

Course Code: 17EC743

CO	Assignment 1	Assignment 2	Assignment 3
C404.1	Y		
C404.2	Y		
C404.3			Y
C404.4		Y	
C404.5		Y	Y

Sl.No	USN	NAME	Assignment1	Assignment 2	Assignment 3
1	3VC16EC011	MONISHA B S	5	5	5
2	3VC16EC033	HARITHA	5	5	5
3	3VC16EC065	RAGHAVENDRA	5	5	5
4	3VC16EC098	UDAY GEETH RAJ	5	5	5
5	3VC17EC004	ANJUM K M	5	5	5
6	3VC17EC009	BHAVANI	5	5	5
7	3VC17EC015	CHETANA GUMASTE	5	5	5
8	3VC17EC016	DIVYASHREE	5	5	5
9	3VC17EC018	GAGANA B J	5	5	5
10	3VC17EC022	JAIPRAKASH N	5	5	5
11	3VC17EC023	JYOTHI H	5	5	5
12	3VC17EC024	K SUSHMA	5	5	5
13	3VC17EC025	K SWETHA	5	5	5
14	3VC17EC027	KEERTHI M V	5	5	5
15	3VC17EC031	MANASA B	5	5	5
16	3VC17EC033	MANJUNATH SUNKAD	5	5	5
17	3VC17EC035	MEGHANA R	5	5	5
18	3VC17EC036	N SOWBAGYASHREE	5	5	5
19	3VC17EC038	NAYUM PASHA	5	5	5
20	3VC17EC039	NEELESH PATIL	5	5	5
21	3VC17EC044	PAWAN KUMAR M	5	5	5
22	3VC17EC047	PRAVEEN KUMAR GOTUR	5	5	5
23	3VC17EC050	RAJASHEKAR REDDY S	5	5	5
24	3VC17EC051	RAJU GHEEWARI	5	5	5
25	3VC17EC055	S KIRAN KUMAR	5	5	5
26	3VC17EC060	SAI KRISHNA BURUGUPALLI	5	5	5
27	3VC17EC061	SAI KRISHNA M	5	5	5
28	3VC17EC062	SEEMA P	5	5	5
29	3VC17EC069	SONIA	5	5	5
30	3VC17EC071	SOUNDARYA V S	5	5	5
31	3VC17EC073	M SUCHITHA	5	5	5
32	3VC17EC076	TEJASHWINI M	5	5	5

33	3VC17EC078	TRIVENI	5	5	5
34	3VC17EC079	VENKATESH K	5	5	5
35	3VC17EC081	VINAYAKA V	5	5	5
36	3VC18EC402	RAGHAVENDRA KM	5	5	5
37					
38					
39					
40					
41					
42					
43					
44					
59					
60					
		Marks scored	180	180	180
		no of students Attempted	36	36	36
		[illegible]	36	36	36
		[illegible]	100	100	100
		Average	1.00	1.00	1.00

CO	Assignment-1	Assignment-2	Assignment-3	Average
C404.1	1.00			1.00
C404.2	1.00			1.00
C404.3			1.00	1.00
C404.4		1.00	1.00	1.00
C404.5		1.00	1.00	1.00

COURSE EXIT SURVEY 2020-21

Faculty: Phanindra Reddy K Course Name: Real Time Systems

C404.1	Explain the fundamentals of real time systems, its classification and Understand the concepts of computer control
C404.2	Describe computer hardware requirement for real time applications
C404.3	Summarize programming language basics for real time application
C404.4	Describe the operating system concepts and techniques required for real time
C404.5	Explain various methodologies used for designing a real time system

SI NO.	USN	Student name	C404.1	C404.2	C404.3	C404.4	C404.5
1	3VC16EC011	MONISHA B S	5	5	5	5	5
2	3VC16EC033	HARITHA	5	5	5	5	5
3	3VC16EC065	RAGHAVENDRA	5	5	5	5	5
4	3VC16EC098	UDAY GEETH RAJ	5	5	5	5	4
5	3VC17EC004	ANJUM K M	5	5	4	5	5
6	3VC17EC009	BHAVANI	5	5	5	5	5
7	3VC17EC015	CHETANA GUMASTE	5	5	5	5	5
8	3VC17EC016	DIVYASHREE	5	5	5	5	5
9	3VC17EC018	GAGANA B J	5	5	5	5	5
10	3VC17EC022	JAIPRAKASH N	5	5	5	5	5
11	3VC17EC023	JYOTHI H	5	5	5	5	5
12	3VC17EC024	K SUSHMA	4	5	5	5	5
13	3VC17EC025	K SWETHA	5	5	4	5	5
14	3VC17EC027	KEERTHI M V	5	5	5	5	5
15	3VC17EC031	MANASA B	5	5	5	4	5
16	3VC17EC033	MANJUNATH SUNKAD	5	5	5	5	5
17	3VC17EC035	MEGHANA R	5	5	5	5	5
18	3VC17EC036	N SOWBAGYASHREE	5	5	5	5	5
19	3VC17EC038	NAYUM PASHA	5	5	5	4	5
20	3VC17EC039	NEELESH PATIL	5	5	5	5	5
21	3VC17EC044	PAWAN KUMAR M	5	5	5	5	5
22	3VC17EC047	PRAVEEN KUMAR GOTUR	5	4	5	5	5
23	3VC17EC050	RAJASHEKAR REDDY S	5	5	5	5	5
24	3VC17EC051	RAJU GHEEWARI	5	5	5	5	5
25	3VC17EC055	S KIRAN KUMAR	4	5	4	5	4
26	3VC17EC060	SAI KRISHNA BURUGUPALLI	5	5	5	5	5
27	3VC17EC061	SAI KRISHNA M	5	5	5	5	5
28	3VC17EC062	SEEMA P	5	5	5	5	4
29	3VC17EC069	SONIA	4	5	5	5	5
30	3VC17EC071	SOUNDARYA V S	5	5	5	5	5
31	3VC17EC073	M SUCHITHA	5	5	5	5	5
32	3VC17EC076	TEJASHWINI M	4	5	5	5	5
33	3VC17EC078	TRIVENI	5	5	5	5	5
34	3VC17EC079	VENKATESH K	5	5	5	5	5
35	3VC17EC081	VINAYAKA V	5	5	5	4	5
36	3VC18EC402	RAGHAVENDRA KM	5	4	5	5	5
		AVERAGE	4.89	4.94	4.92	4.92	4.92
			0.98	0.99	0.98	0.98	0.98
		% CO Attainment	98	99	98	98	98
		ATTAINMENT LEVEL	3	3	3	3	3

RTS SELF ASSESSMENT REPORT 2020-21

Faculty **Phanindra Reddy K** Sem **7**

17EC743 Sec **A**

Q1	Are you able to define real time system?
Q2	Are you able to understand sequence control?
Q3	Are you able to explain pulse interface
Q4	Are you able to list requirement of programming language
Q5	Are you able to explain exception handling
Q6	Are you able to explain scheduling strategies
Q7	Are you able to explain why we use RTOS
Q8	Are you able to undertsand planning and development phase of RTS
Q9	Are you able to describe major methodologies
Q10	Are you able to understand process specification and control specification

CO	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
C404.1	y	y								
C404.2			y							
C404.3				y	y					
C404.4						y	y			
C404.5								y	y	y

R NO	USN	Student name	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
1	3VC16EC011	MONISHA B S	5	5	5	5	5	5	5	5	5	5
2	3VC16EC033	HARITHA	5	5	5	5	5	5	5	5	5	5
3	3VC16EC065	RAGHAVENDRA	5	5	5	5	5	5	5	5	5	5
4	3VC16EC098	UDAY GEETH RAJ	5	5	5	5	4	5	5	5	5	4
5	3VC17EC004	ANJUM K M	5	5	4	5	5	5	5	4	5	5
6	3VC17EC009	BHAVANI	5	5	5	5	5	5	5	5	5	5
7	3VC17EC015	CHETANA GUMASTE	5	5	5	5	5	5	5	5	5	5
8	3VC17EC016	DIVYASHREE	5	5	5	5	5	5	5	5	5	5
9	3VC17EC018	GAGANA B J	5	5	5	5	5	5	5	5	5	5
10	3VC17EC022	JAIPRAKASH N	5	5	5	5	5	5	5	5	5	5
11	3VC17EC023	JYOTHI H	5	5	5	5	5	5	5	5	5	5
12	3VC17EC024	K SUSHMA	4	5	5	5	5	4	5	5	5	5
13	3VC17EC025	K SWETHA	5	5	4	5	5	5	5	4	5	5
14	3VC17EC027	KEERTHI M V	5	5	5	5	5	5	5	5	5	5
15	3VC17EC031	MANASA B	5	5	5	4	5	5	5	5	4	5
16	3VC17EC033	MANJUNATH SUNKAD	5	5	5	5	5	5	5	5	5	5
17	3VC17EC035	MEGHANA R	5	5	5	5	5	5	5	5	5	5
18	3VC17EC036	N SOWBAGYASHREE	5	5	5	5	5	5	5	5	5	5
19	3VC17EC038	NAYUM PASHA	5	5	5	4	5	5	5	5	4	5
20	3VC17EC039	NEELESH PATIL	5	5	5	5	5	5	5	5	5	5
21	3VC17EC044	PAWAN KUMAR M	5	5	5	5	5	5	5	5	5	5
22	3VC17EC047	PRAVEEN KUMAR GOTUR	5	4	5	5	5	5	4	5	5	5
23	3VC17EC050	RAJASHEKAR REDDY S	5	5	5	5	5	5	5	5	5	5
24	3VC17EC051	RAJU GHEEWARI	5	5	5	5	5	5	5	5	5	5
25	3VC17EC055	S KIRAN KUMAR	4	5	4	5	4	4	5	4	5	4
26	3VC17EC060	SAI KRISHNA BURUGUPALLI	5	5	5	5	5	5	5	5	5	5

R NO	USN	Student name	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
27	3VC17EC061	SAI KRISHNA M	5	5	5	5	5	5	5	5	5	5
28	3VC17EC062	SEEMA P	5	5	5	5	4	5	5	5	5	4
29	3VC17EC069	SONIA	4	5	5	5	5	4	5	5	5	5
30	3VC17EC071	SOUNDARYA V S	5	5	5	5	5	5	5	5	5	5
31	3VC17EC073	M SUCHITHA	5	5	5	5	5	5	5	5	5	5
32	3VC17EC076	TEJASHWINI M	4	5	5	5	5	4	5	5	5	5
33	3VC17EC078	TRIVENI	5	5	5	5	5	5	5	5	5	5
34	3VC17EC079	VENKATESH K	5	5	5	5	5	5	5	5	5	5
35	3VC17EC081	VINAYAKA V	5	5	5	4	5	5	5	5	4	5
36	3VC18EC402	RAGHAVENDRA KM	5	4	5	5	5	5	4	5	5	5
		Average	4.89	4.944	4.92	4.917	4.92	4.89	4.9	4.92	4.92	4.92
		CO Attainment	0.98	0.99	0.98	0.98	0.98	0.98	0.99	0.98	0.98	0.98
		%CO Attainment	97.8	98.9	98.3	98.3	98.3	97.8	98.9	98.3	98.3	98.3

C404.1	0.98	0.99									0.98
C404.2			0.98								0.98
C404.3				0.98	0.98						0.98
C404.4						0.98	0.99				0.98
C404.5								1	1	0.98	0.98

RAO BAHADUR Y MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARIDEPARTMENT OF ELECTRONICS COMMUNICATION ENGNEERING

DIRECT & INDIRECT ATTAINMENT 2020-21

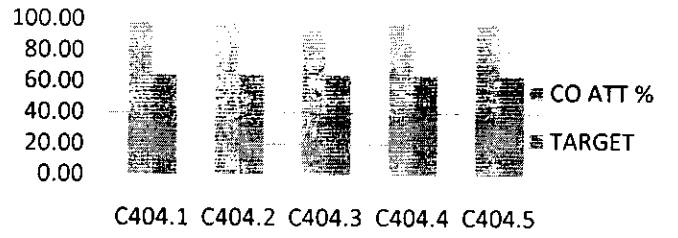
Faculty: Phanindra Reddy K					
Course Name: Real Time Systems					
Course Code: 17EC743	**Sem**	**7**	**Sec**	**A**	
C404.1	Explain the fundamentals of real time systems, its classification and Understand the concepts of computer control				
C404.2	Describe computer hardware requirement for real time applications				
C404.3	Summarize programming language basics for real time application				
C404.4	Describe the operating system concepts and techniques required for real time system				
C404.5	Explain various methodologies used for designing a real time system				

CO-PO/PSO Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
C404.1	3													
C404.2	3	2												
C404.3	3	2												
C404.4	3	2												
C404.5	2		2											
AVG	3	2.5	3											

CO DIRECT & INDIRECT ATTAINMENT

	CO AT	TARGET
C404.1	98.17	65
C404.2	98.28	65
C404.3	94.81	65
C404.4	98.19	65
C404.5	98.19	65



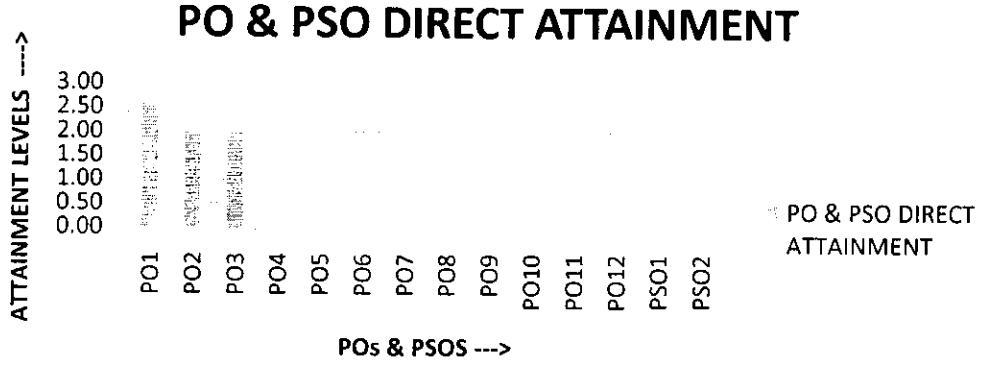
PO & PSO DIRECT ATTAINMENT

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
PO ATT	2.80	2.00	2.00											

PO & PSO INDIRECT ATTAINMENT

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
PO ATT	2.80	2.00	2.00											

PO & PSO DIRECT ATTAINMENT



RAO BAHADUR Y. MAHABALESWARAPPA ENGINEERING COLLEGE, BALLARI
Department of Electronics and Communication Engineering

RTS 7A

CO ATTAINMENT GAP ANALYSIS 2020-21

17EC743

Course Outcomes	CO Direct Attainment	CO Target	CO Attainment Gap
C404.1	98.17	65	NIL
C404.2	98.28	65	NIL
C404.3	94.81	65	NIL
C404.4	98.19	65	NIL
C404.5	98.19	65	NIL

ACTION REPORT ON GAP ANALYSIS

Course Outcomes	Action proposed to bridge the gap	Modification of target if achieved
C404.1	NIL	67
C404.2	NIL	67
C404.3	NIL	67
C404.4	NIL	67
C404.5	NIL	67

Modified

CBCS SCHEME

USN | | | | | | | | | | |

17EC743

Seventh Semester B.E. Degree Examination, Jan./Feb. 2021
Real Time Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Real Time System. Explain different classification of Real Time System with example. **(08 Marks)**

b. Explain computer control system showing hardware and software interface. **(06 Marks)**

c. Discuss different types of programs in system design. **(06 Marks)**

OR

2 a. Explain sequence control for single chemical reactor vessel with diagram. **(08 Marks)**

b. Explain the following: i) Batch process ii) Continuous process. **(06 Marks)**

c. Write a short note on hierarchical system. **(06 Marks)**

Module-2

3 a. Explain Digital input and output Interface with diagrams. **(10 Marks)**

b. Explain different forms of parallel computer architectures. **(10 Marks)**

OR

4 a. Explain daisy chains interrupt structure. **(08 Marks)**

b. Write a note on multilevel interrupts. **(06 Marks)**

c. Discuss Asynchronous and Synchronous Transmission techniques. **(06 Marks)**

Module-3

5 a. Explain the following: i) Security ii) Readability iii) Portability iv) Efficiency. **(10 Marks)**

b. Discuss different data types with example. **(10 Marks)**

OR

6 a. Explain briefly declaration and initialization of variables and constants. **(08 Marks)**

b. Write a short note on exception handling. **(06 Marks)**

c. Explain Coroutines. **(06 Marks)**

Module-4

7 a. Explain typical structure of Real time operating system with diagram. **(08 Marks)**

b. Describe different types of scheduling strategies. **(06 Marks)**

c. Explain task chaining and swapping with diagram. **(06 Marks)**

OR

8 a. Explain general structure of Input output subsystem. **(08 Marks)**

b. Explain: i) Serially reusable code ii) Re-entrant code. **(06 Marks)**

c. Write a note on monitors. **(06 Marks)**

Module-5

9 a. Explain planning phase and development phase related to design of Real time system. **(10 Marks)**

b. Describe foreground background approach with reference to Real time system design. **(10 Marks)**

OR

10 a. Explain context diagram for drying oven in case of Ward and Mellor method. **(06 Marks)**

b. Differentiate between Ward and Mellor and Hatley and Pirbhai methodologies. **(06 Marks)**

c. Explain requirement model in case of Hatley and Pirbhai method. **(08 Marks)**

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