	RaoBahadur Y Mahabaleswarappa Engineering College, Cantonment, Ballari.	RECORD FORMATS (ISO 9001:2008) *W.E.F:* 2/9/2019	
	Dept. of Electronics & Communication Engineering	ODD Semester Time Table-2019-20	

SEM: III A **Branch Code: EC** **Room No. : 201 (MAIN BUILDING)**

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	ED	COA	BREAK	M-III	DSD	LUNCH BREAK	EDI/DSD LAB NT-Tutorial		
TUE	NT	PE & I		ED	COA		EDI/DSD LAB NT-Tutorial		
WED	DSD	NT		M-III	COA		EDI/DSD LAB NT-Tutorial		
THU	COA	ED		DSD	M-III		PE & I	NT	DSD
FRI	PE & I	DSD		NT	ED		COA	PE & I	M-III
SAT	M-III	ED		PE & I	NT				

Class Coordinator: Mr. Srikanth N

Subject	Sub Code	Faculty Incharge	Subject	Sub Code	Faculty Incharge
Mathematics	18MAT31	Mrs. Ambika	Computer Organization & Architecture	18EC35	Mrs. Chinna V Gowdar
Network Theory	18EC32	Dr. Shivakumar	Power Electronics & Instrumentation	18EC36	Mrs.Girija Vani
Electronic Devices	18EC33	Mr. Khaja Moinuddin	Electronic Devices & Instrumentation Lab	18ECL37	Dr. Shivakumar/Mr. Khaja Moinuddin/Rohini H M
Digital System Design	18EC34	Mr. Srikanth N	Digital System Design Lab	18ECL38	Mr. Srikanth N/ Mr. Vinay A
CIP	18CPC39	Mr.. Dalal Shivakumar	Additional Mathematics- I	18MATDIP31	Dr. J Phakirappa
Network Theory (T)	18EC32	Mrs. Vani H			

Signature:
Timetable Cordinators:Mrs.Suvarna S Patil/ Mrs.Chinna V Gowdar
Designation: Asst.Prof/Asst.Prof

Head of the Department
Electronics & Communication Engg.
R.Y.M. Engineering College
(Formerly Vijayanagar Engg. College)
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Signature:
Approved by: Dr. Sangeeta. Sololi
Designation: HOD

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	RaoBahadur Y Mahabaleswarappa Engineering College, Cantonment, Ballari.	RECORD FORMATS (ISO 9001:2008)*W.E.F: 5/08/2019*
	Dept. of Electronics & Communication Engineering	**ODD Semester Time Table-2019-20**

SEM: III B **Branch Code: EC** **Room No. : 202 (MAIN BUILDING)**

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	NT	DSD	BREAK	ED	PE & I	LUNCH BREAK	M-III	COA	PE & I
TUE	M-III	PE & I		COA	ED		NT	DSD	ED
WED	ED	COA		NT	DSD		COA	M-III	NT
THU	PE & I	ED		COA	M-III		EDI/DSD LAB NT-Tutorial		
FRI	NT	M-III		DSD	PE & I		EDI/DSD LAB NT-Tutorial		
SAT	DSD	EDI/DSD LAB NT-Tutorial							

Class Coordinator: Mr. Md. Zakirulla

Subject	Sub Code	Faculty Incharge	Subject	Sub Code	Faculty Incharge
Mathematics	18MAT31	Dr. Shruti .R	Computer Organization & Architecture	18EC35	Mr. Lokesh K S
Network Theory	18EC32	Mr. Sharana Basavaraj B	Power Electronics & Instrumentation	18EC36	Mr. Md. Zakirulla
Electronic Devices	18EC33	Mrs. Vani H	Electronic Devices & Instrumentation Lab	18ECL37	Dr. Prabhavathi/Mrs. Vani H
Digital System Design	18EC34	Mr. Shridhar S.B	Digital System Design Lab	18ECL38	Mr. Dalal Shivakumar/ Mr. Shridhar S.B
CIP	18CPC39	Mr. Dalal Shivakumar	Additional Mathematics- I	18MATDIP3	Dr. J Phakirappa
Network Theory (T)	18EC32	Mr. Sharana Basavaraj B			

Signature:
Timetable Cordinators:Mrs.Suvarna S Patil/ Mrs.Chinna V Gowdar
Designation: Asst.Prof/Asst.Prof

Signature: Head of the Department
Approved by: Dr. Savita Sololi
Designation: HOD
Dept. of Electronics & Communication Engg
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	RaoBahadur Y Mahabaleswarappa Engineering College, Cantonment, Ballari.	**RECORD FORMATS (ISO 9001:2008)*W.E.F: 5/08/2019***
	Dept. of Electronics & Communication Engineering	**ODD Semester Time Table-2019-20**

SEM: V A **Branch Code: EC** **Room No. : 102 (MAIN BUILDING)**

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	Verilog HDL	Oops/8051	BREAK	M&E	ITC	LUNCH BREAK	DSP	OS	M&E
TUE	DSP	OS		Verilog HDL	M&E		ITC	Verilog HDL	OS
WED	OS	Verilog HDL		Oops/8051	DSP		M&E	ITC	
THU	M&E	Verilog HDL		ITC	Oops/8051		DSP LAB /HDL LAB		
FRI	ITC	OS		Oops/8051	DSP		DSP LAB /HDL LAB		
SAT	Oops/8051	DSP	DSP LAB /HDL LAB						

Class Coordinator: Mrs. Vani H

Subject	Sub Code	Faculty Incharge	Subject	Sub Code	Faculty Incharge
Management &Enterpreneur (M&E)	17EC51	Mr. Dalal Shivakumar	Operating System	17EC553	Mr Channaveerana Gouda
Digital Signal Processing (DSP)	17EC52	Mr. Srikanth N	OOPs/ MC 8051	17EC562 17EC563	Mr. K.P.Reddy Mr. Veerareddy
Verilog HDL	17EC53	Dr. Savita Sonoli	DSP Lab	17ECL57	Mrs. Suvarna Patil/ Mrs.Girija Vani
Information Theory & Coding (ITC)	17EC54	Mrs. Suvarna Patil	HDL Lab	17ECL58	Mr. Veerareddy/ Mr. Prashanth K

Signature:
Timetable Cordinators:Mrs.Suvarna S Patil/ Mrs.Chinna V Gowdar
Designation: Asst.Prof/Asst.Prof

Signature:
Approved by: Dr. Savita. Sonoli
Designation: HOD

Head of the Department
Electronics & Communication Engg.
R.Y.M. Engineering College
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	RaoBahadur Y Mahabaleswarappa Engineering College, Cantonment, Ballari.	RECORD FORMATS (ISO 9001:2008)*W.E.F: 5/08/2019*
	Dept. of Electronics & Communication Engineering	**ODD Semester Time Table-2019-20**

SEM: V B **Branch Code: EC** **Room No. : 203 (MAIN BUILDING)**

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	DSP	Oops/8051	BREAK	ITC	M&E	LUNCH BREAK	DSP LAB /HDL LAB		
TUE	OS	Verilog HDL		M&E	OS		DSP LAB /HDL LAB		
WED	Verilog HDL	DSP		Oops/8051	ITC		DSP LAB /HDL LAB		
THU	ITC	M&E		ITC	Oops/8051		Verilog HDL	OS	M&E
FRI	M&E	Verilog HDL		Oops/8051	DSP		ITC	DSP	OS
SAT	Oops/8051	DSP		Verilog HDL	OS				

Class Coordinator: Mr. Shridhar S.B

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Management &Entrepreneur (M&E)	17EC51	Mr. Shridhar S.B	Operating System	17EC551	Mr. K.P.Reddy
Digital Signal Processing (DSP)	17EC52	Mr. Surendranath H	OOPs/ MC 8051	17EC562 17EC563	Mr. K.P.Reddy Mr. Veerareddy
Verilog HDL	17EC53	Mrs. Chinna V Gowdar	DSP Lab	17ECL57	Mrs. Rakhee Patil/Mr. Surendranath.H
Information Theory &Coding(ITC)	17EC54	Dr. Prabhavathi .S	HDL Lab	17ECL58	Mrs. Anitha A/ Mr. Sudarshan B

Signature: **Timetable Cordinators:Mrs.Suvarna S Patil/ Mrs.Chinna V Gowdar** **Designation: Asst.Prof/Asst.Prof**	Signature: **Approved by: Dr. Savita Sonoli** **Designation: HOD**	PRINCIPAL R.Y.M. Engineering College. (Formerly Vijayanagar Engg. College) Cantonment, BELLARY-583 104

	RaoBahadur Y Mahabaleswarappa Engineering College, Cantonment, Ballari.	**RECORD FORMATS (ISO 9001:2008)*W.E.F: 5/08/2019***
	Dept. of Electronics & Communication Engineering	**ODD Semester Time Table-2019-20**

SEM: VII A **Branch Code: EC** **Room No. : 204 (MAIN BUILDING)**

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	RTS	ADC/VLSI Lab				LUNCH BREAK	DIP	IoT&WSN	PE
TUE	DIP	ADC/VLSI Lab					PE	M&A	RTS
WED	M&A	ADC/VLSI Lab					M&A	DIP	IoT&WSN
THU	IoT&WSN	PE	BREAK	M&A	DIP		RTS	Project Work	
FRI	RTS	M&A		IoT&WSN	PE		Project Work		
SAT	PE	RTS		IoT&WSN	DIP				

Class Coordinator: Mr. Lokesh K S

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Microwave &Antennas (M&A)	15EC71	Mr. Md. Zakirulla	IOT & Wireless Sensor Networks	15EC752	Mr. Prashanth K
Digital Image Processing(DIP)	15EC72	Mr. Surendranath H	Advanced Communication Lab	15ECL76	Mr. K.P Reddy/ Mr. S. V Patil
Power Electronics (PE)	15EC73	Mr. S. V Patil	VLSI Lab	15ECL77	Mr. Lokesh K S/ Mr. Veerareddy
Real Time Systems(RTS)	15EC743	Mr. Lokesh K S	Project Work Phase-I	15ECP78	Mr. Vinay A

Signature: **Timetable Cordinators:Mrs.Suvarna S Patil/ Mrs.Chinna V Gowdar** **Designation: Asst.Prof/Asst.Prof**	Signature: **Approved by: Dr. Savita Sonoli** **Designation: HOD** Head of the Department Dept. of Electronics & Communication Engg. R.Y.M. Engineering College (Formerly Vijayanagar Engg. College) BELLARY-583 104	PRINCIPAL R.Y.M. Engineering College. (Formerly Vijayanagar Engg. College) Cantonment, BELLARY-583 104

	RaoBahadur Y Mahabaleswarappa Engineering College, Cantonment, Ballari.	RECORD FORMATS (ISO 9001:2008)*W.E.F: 5/08/2019*	
	Dept. of Electronics & Communication Engineering	ODD Semester Time Table-2019-20	

SEM: VII B **Branch Code: EC** **Room No. : 205 (MAIN BUILDING)**

DAY	9.00am-9.55am	9.55am-10.50am	10.50am - 11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	DIP	IoT&WSN	BREAK	RTS	PE	LUNCH BREAK	M&A	Project Work	
TUE	RTS	M&A		IoT&WSN	DIP		Project Work		
WED	M&A	RTS		PE	IoT&WSN		DIP	M&A	PE
THU	IoT&WSN	ADC/VLSI Lab					PE	RTS	M&A
FRI	PE	ADC/VLSI Lab					IoT&WSN	DIP	RTS
SAT	ADC/VLSI Lab				DIP				

Class Coordinator: Ms. Rohini H M

Subject	Sub Code	Faculty Incharge	Subject	Sub Code	Faculty Incharge
Microwave &Antennas(M&A)	15EC71	Mrs. Anitha A	IOT & Wireless Sensor Networks	15EC752	Mrs. Suvarna Patil
Digital Image Processing(DIP)	15EC72	Ms. Rohini H M	Advanced Communication Lab	15ECL76	Mr. Sudharshan B
Power Electronics (PE)	15EC73	Mrs. Rakhee Patil	VLSI Lab	15ECL77	Dr. Savita Sonoli/ Mrs. Chinna V Gowdar/ Sharana Basavaraj B
Real Time Systems(RTS)	15EC743	Mr. Khaja Moinuddin	Project Work Phase-I	15ECP78	Dr. Prabhavathi .S / ASHWINI.K

Signature:
Timetable Cordinators:Mrs.Suvarna S Patil/ Mrs.Chinna V Gowdar
Designation: Asst.Prof/Asst.Prof

Signature:
Approved by:Dr. Savita Sonoli
Designation: HOD
Head of the Department
Electronics & Communication Engg.
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3/8/19

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