



SEM: IV A

Branch Code: EC

Room No. : 201(MAINBUILDING)

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm	
MON	LIC	MP	BREAK	PCS	CS	LUNCH BREAK	MP LAB/LIC+COMM LAB			
								CS(T)	S&S(T)	
TUE	CS	LIC		MP	M-IV			MP LAB/LIC+COMM LAB		
								S&S(T)	CS(T)	
WED	S&S	CS		M-IV	MP			MP LAB/LIC+COMM LAB		
								CS(T)	S&S(T)	
THU	PCS	M-IV		LIC	S&S			PCS	MP	CS
FRI	MP	M-IV		CS	S&S			S&S	LIC	PCS
SAT	M-IV	PCS	S&S	LIC		Kannada Kali/Manasu				

Class Coordinator: Mr. Manjunath K.M

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Maths-IV	17MAT41	Mr. Manjunath	Linear Integrated Circuits (LIC)	17EC45	Mr. Nalavadi Srikantha
Signals & Systems(S&S)	17EC42	Mrs. Vani H	Microprocessor (MP)	17EC46	Mr. Manjunath K.M.
Control System (CS)	17EC43	Mr. Sharana Basavaraj B	Microprocessor Lab (MP Lab)	17ECL47	Mr. Manjunath K.M / Mrs. Vani H
Principles of Communication Systems (PCS)	17EC44	Mr. Lokesh.K.S/ Mr. Nalavadi Srikantha	LIC+ Communication Lab (LIC+Comm)	17ECL48	Mr. Nalavadi Srikantha / Mr. Sharana Basavaraj B
Kannada Kali/Manasu	17KL49	Mrs. Vani H			
Signals & Systems(S&S)(T)	17EC42	Mr. Santosh M	Control System (CS)(T)	17EC43	Sudarshan B

Signature:
Timetable Cordinators: Designation: Mrs. Suvarna Patil
Asst.Prof / Mrs. Chinnappa V Gowdar Asst.Prof
/ Mr. R. Pawan Kumar Asst.Prof

Signature: Head of the Department.
Approved by: Dr. Savitha Sogoli
Designation: Professor & Vice Principal
Formerly Vijayanagar Engg. College
BELLARY-583 104

PRINCIPAL
PRINCIPAL
R.Y.M. Engineering College.
(Formerly Vijayanagar Engg. College)
Cantonment, BELLARY-583 104



**Rao Bahadur Y Mahabaleswarappa Engineering College,
Cantonment, Ballari.**

**RECORD FORMATS
(ISO 9001:2008)W.E.F:01/02/19**



Dept. of Electronics & Communication Engineering

EVEN Semester Time Table

SEM: IV B

Branch Code: EC

Room No. : 202(MAIN BUILDING)

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm	
MON	MP	S&S	BREAK	PCS	M-IV	LUNCH BREAK	LIC	CS	MP	
TUE	S&S	LIC		CS	MP		M-IV	PCS	LIC	
WED	LIC	CS		S&S	PCS		S&S	MP	M-IV	
THU	M-IV	MP		CS	S&S		MP LAB/LIC+COMM LAB		CS(T)	S&S(T)
FRI	CS	M-IV		LIC	PCS		MP LAB/LIC+COMM LAB		S&S(T)	CS(T)
SAT	PCS	MP LAB/LIC+COMM LAB			Kannada Kali/Manasu					
		CS(T)		S&S(T)						

Class Coordinator: Mr.R Pawankumar

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Maths-IV	17MAT41	Mr.Shaikshavali	Linear Integrated Circuits (LIC)	17EC45	Mr. Dalal Shivakumar
Signals & Systems(S&S)	17EC42	Dr. Prabhavathi S	Microprocessor (MP)	17EC46	Mr. Shridhar S Bilagi
Control System (CS)	17EC43	Dr. Shivakumar S B	Microprocessor Lab (MP Lab)	17ECL47	Mr. Shridhar S Bilagi / Mr. Md. Zakirulla
Principles of Communication System(PCS)	17EC44	Mr.Pawan Kumar R	LIC+ Communication Lab (LIC+Comm)	17ECL48	Mr. Dalal Shivakumar /Mr. Sudharshan Banakar
Kannada Kali/Manasu	17KL49	Mrs. Vani H			
Signals & Systems(S&S)(T)	17EC42	Mr. Manjunath K.M.	Control System (CS)(T)	17EC43	Mr. A Vinay

Signature:

**Timetable Cordinators: Designation:Mrs.Suvarna Patil
Asst.Prof /MrsChinna V Gowdar Asst.Prof
/Mr.R.PawanKumar Asst.Prof**

Head of the Department.

Signature:
Approved by: **Dr. Savita Sonoli**
Designation: **Professor & Vice Principal**
BELLARY-583 104

PRINCIPAL
R.Y.M. **PRINCIPAL** College,
(Formerly Vijayanagar Engg. College)
Cantonment, BELLARY-583 104



**Rao Bahadur Y Mahabaleswar Engineering College,
Cantonment, Ballari.**

**RECORD FORMATS
(ISO 9001:2008)W.E.F:01/02/19**



Dept. of Electronics & Communication Engineering

EVEN Semester Tentative Time Table

SEM: VI A

Branch Code: EC

Room No. : 102 (MAIN BUILDING)

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	DSS	DSDV	BREAK	DC	CCN	LUNCH BREAK	VLSI	CCN	ARM
TUE	ARM	DSDV		VLSI	CCN		DC	ARM	DSS
WED	CCN	VLSI		DSDV	ARM		DSS	VLSI	DSDV DC
THU	DC	CCN		VLSI	DSS		Embedded Controller LAB/ Computer Network LAB		
FRI	DC DSDV	ARM		DSS	DC		Embedded Controller LAB/ Computer Network LAB		
SAT	Embedded Controller LAB/ Computer Network LAB				PLACEMENT TRAINING				

Class Coordinator: Mr.Veerareddy

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Digital Communication	15EC61	Mr. Sharanagouda.V. Patil	Digital Switching System	15EC651	Mr. Surendranath.H
ARM MC &EMD Sys	15EC62	Mr. Veera Reddy	DSDV	15EC663	Dr. Savita Sonoli
VLSI Design	15EC63	Mr. Lokesh.K.S	Embedded Controller Lab	15ECL67	Mr. Veera Reddy/ Mr. Santosh M
Computer Comm Network	15EC64	Dr. Prabhavathi S/ Mr. K.P.Reddy	Computer Network Lab	15ECL68	Mr. K.P.Reddy/ Mr. Nagaraj Gouda

Signature:

**Timetable Cordinators: Designation: Mrs. Suvarna Patil
Asst.Prof /MrsChinna Gowdar Asst.Prof
/Mr.R.PawanKumar Asst.Prof**

Signature: *[Signature]*
Head of the Department
Approved by: Dr. Savitha Sonoli
Designation: Professor & Vice Principal

PRINCIPAL

[Signature]
31/1/19
PRINCIPAL
R.Y.M. Engineering College,
(Formerly Vijayanagar Engg. College),
Cantonment, BELLARY-583 104

BELLARY-583 104



Rao Bahadur Y Mahabaleswara Engineering College,
Cantonment, Ballari.

RECORD FORMATS
(ISO 9001:2008)W.E.F:01/02/19



Dept. of Electronics & Communication Engineering

EVEN Semester Tentative Time Table

SEM: VI B

Branch Code: EC

Room No. : 204 (MAIN BUILDING)

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	DSS	VLSI	BREAK	DC	CCN	LUNCH BREAK	Embedded Controller LAB/ Computer Networks LAB		
TUE	DC	VLSI		ARM	DSDV		Embedded Controller LAB/ Computer Networks LAB		
WED	VLSI	DC		ARM	DSS		Embedded Controller LAB/ Computer Networks LAB		
THU	ARM	DSS		CCN	DSDV		DC	CCN	VLSI
FRI	DSDV	CCN		DSS	ARM		DSDV	DSS	ARM
SAT	CCN	VLSI		DC	PLACEMENT TRAINING				

Class Coordinator: Mr.Channaveerana Gouda

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Digital Communication	15EC61	Mrs.A Anitha	Digital Switching System	15EC651	Ms. Manasa K C
ARM MC &EMD Sys	15EC62	Mr. Khaja Moinuddin	DSDV	15EC663	Mrs. Chinna V Gowdar / Channaveerana Gouda
VLSI Design	15EC63	Mrs. Chinna V Gowdar	Embedded Controller Lab	15ECL67	Mr. Khaja Moinuddin/ Mr. Prashanth K Y
Computer Comm Network	15EC64	Mrs. Suvarna S Patil	Computer Network Lab	15ECL68	Mrs. Suvarna S Patil/ Mr. Channaveerana Gouda

Signature:
Timetable Cordinators: Designation: Mrs. Suvarna Patil
Asst.Prof / Mrs Chinna V Gowdar Asst.Prof
/ Mr.R.PawanKumar Asst.Prof

Head of the Department
Signature: Electronics & Communication Engg.
Approved by: Dr. Santhia Srinivas
Designation: Professor & Vice Principal
BELLARY-583 104

PRINCIPAL
R.Y.M. Engineering College.
(Formerly Vijayanagar Engg. College).
Cantonment. BELLARY-583 104

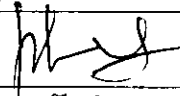



SEM: VIII A


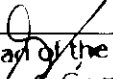
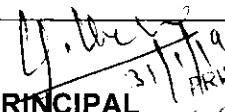
Branch Code: EC

Room No. : 203 (MAIN BUILDING)

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	WC<E	FON	BREAK	SP/ML	SP/ML	LUNCH BREAK	SEMINAR		
TUE	SP/ML	WC<E		FON	FON		SEMINAR		
WED	FON	SP/ML		WC<E	WC<E		SEMINAR		
THU	FON	SP/ML		WC<E			PROJECT WORK		
FRI	PROJECT WORK			PROJECT WORK			PROJECT WORK		
SAT									

Class Coordinator: Mr.Sharnagouda V Patil

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Wireless Cellular and LTE 4G Broadband	15EC81	Mr. K.P.Reddy 	Machine learning	15EC834	Ms. Rohini H M
Fiber Optics & Networks	15EC82	Mr. Md. Zakirulla 	Project Work	15ECP85	Dr. Prabhavathi S/Ms. Rohini H M
Speech Processing	15EC832	Mr. Santosh M 	Seminar	15ECS86	Mr. Surendranath.H /Mr. Lokesh.K.S /Mr. Sharanagouda.V. Patil 

Signature:  Timetable Cordinators Designation: Mrs.Suvarna Patil Asst.Prof /MrsChinna Gowdar Asst.Prof /Mr.R.PawanKumar Asst.Prof	Signature:  Head of the Department, Department of Electronics & Communication Engg Approved by: Dr. Sayitha Sonali Designation: Professor & Vice-Principal Formerly Vijayanagar Engg. College BELLARY-583 104	 PRINCIPAL RYM Engineering College. (Formerly Vijayanagar Engg. College) Cantonment, BELLARY-583 104
--	--	--



Rao Bahadur Y Mahabaleswara Engineering College,
Cantonment, Ballari.

RECORD FORMATS
(ISO 9001:2008) W.E.F:01/02/19



Dept. of Electronics & Communication Engineering

EVEN Semester Tentative Time Table

SEM: VIII B

Branch Code: EC

Room No. : 205 (MAIN BUILDING)

DAY	9.00am-9.55am	9.55am-10.50am	10.50am-11.00am	11.00am-11.55am	11.55am-12.50pm	12.50pm-2.15pm	2.15pm-3.10pm	3.10pm-4.05pm	4.05pm-5pm
MON	WC<E	FON	BREAK	SP/ML	SP/ML	LUNCH BREAK	PROJECT WORK		
TUE	SP/ML	FON		WC<E	WC<E		PROJECT WORK		
WED	FON	SP/ML		WC<E	FON		PROJECT WORK		
THU	FON	SP/ML		WC<E			SEMINAR		
FRI	SEMINAR			SEMINAR			SEMINAR		
SAT									

Class Coordinator: Mrs.Anitha A

Subject	Sub Code	Faculty In charge	Subject	Sub Code	Faculty In charge
Wireless Cellular and LTE 4G Broadband	15EC81	Mrs. Anitha.A/ Mr.S. V Patil	Machine learning <i>Speech Processing</i>	15EC834	Ms. Rohini H M
Fiber Optics & Networks	15EC82	Mr. Channaveerana Goudar	Project Work	15ECP85	Mr. Vinay.A /Mr. Pawan Kumar R
Speech Processing	15EC832	Mr. Santosh M	Seminar	15ECS86	Mrs. Chinna V Gowdar/Mrs. Anitha.A /Ms.Kumuda B

Signature:
Timetable Cordinators: Designation: Mrs. Suvarna Patil
Asst.Prof /Mrs Chinna V Gowdar Asst.Prof
/Mr.R.PawanKumar Asst.Prof

Head of the Department,
Electronics & Communication Engg
Rao Bahadur Y Mahabaleswara Engineering College,
Cantonment, Ballari.
Approved by: Dr. Savitha Sonali
Designation: Professor & Vice Principal

U. Uthappa
21/11/19
PRINCIPAL
R.Y.M. Engineering College,
Cantonment, Ballari.
(Formerly Vijayanagar Engg. College).
BELLARY-583 104